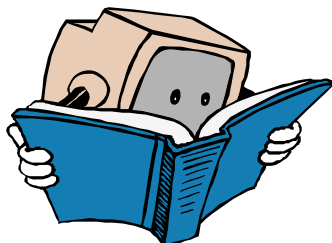


HITACHI

No. 0243



SERVICE MANUAL MANUEL D'ENTRETIEN WARTUNGSHANDBUCH

CAUTION:

Before servicing this chassis, it is important that the service technician read the "Safety Precautions" and "Product Safety Notices" in this service manual.

ATTENTION:

Avant d'effectuer l'entretien du châssis, le technicien doit lire les «Précautions de sécurité» et les «Notices de sécurité du produit» présentés dans le présent manuel.

VORSICHT:

Vor Öffnen des Gehäuses hat der Service-Ingenieur die „Sicherheitshinweise“ und „Hinweise zur Produktsicherheit“ in diesem Wartungshandbuch zu lesen.

32LD8D20E
32LD8D20EA
32LD8D20U
32LD8D20UA
32LD8D20UC
37LD8D20E
37LD8D20U
37LD8D20UA
37LD8D20UC

Data contained within this Service manual is subject to alteration for improvement.

Les données fournies dans le présent manuel d'entretien peuvent faire l'objet de modifications en vue de perfectionner le produit.

Die in diesem Wartungshandbuch enthaltenen Spezifikationen können sich zwecks Verbesserungen ändern.

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SPECIFICATIONS AND PARTS ARE SUBJECT TO CHANGE FOR IMPROVEMENT

Colour Television
December 2007

1. INTRODUCTION

17MB22 Main Board consists of Micronas concept , VCTP as controller. This IC is capable of handling Audio processing, video processing, motion adaptive up conversion(MAU), Scaling-Display processing and FPD control (DPS), unified memory for audio video and Text, 3D comb filter, PC connectivity, OSD and text processing. TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/ G, D/K, I/I' and L/L' including German and NICAM stereo.

Sound system output is supplying 2x 8W (10%THD) for stereo 8Ω speakers
Supported peripherals are:

- 1 RF input VHF1, VHF3, UHF @ 75Ω
- 1 FAV input
- 2 SCART sockets
- 1 SVHS input
- 1 Stereo Headphone input
- 1 YPbPr
- 1 PC input
- 1 HDMI input
- 1 Stereo audio input for PC

2. TUNER

As the thickness of the TV set has a limit, a horizontal mounted tuner is used in the product, which is suitable for CCIR systems B/G, H, L/ L', I/I' and D/ K. The tuning is available through the digitally controlled I2C bus (PLL). Below you will find info on the Tuner in use.

2.1 General description of UV1316

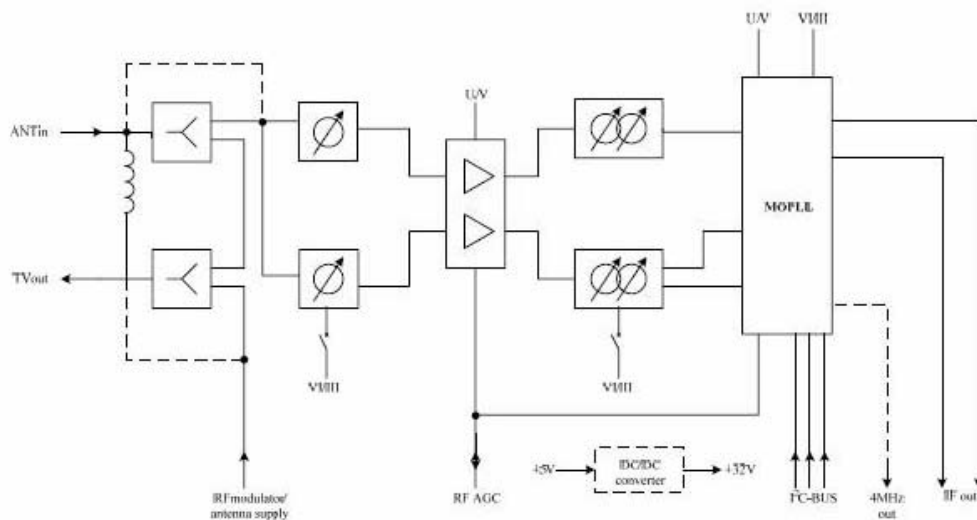
The UV1316 tuner belongs to the UV 1300 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF, UHF tuner suitable for CCIR systems B/G, H, L, L', I and I'. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

2.2 Brief description

The DTT 713XX is designed for digital terrestrial reception in VHFIII and UHF, compliant with the European digital terrestrial standard ETS 300744. In addition it covers all channels from 44.25MHz to 863.25MHz. It is a two band concept, VHF and UHF, with VHF switched between VHF low (VHFI) and VHF high (VHFIII). Optional an antenna loop through function, a combiner to feed through an RF-modulator signal to the TV output, a buffered 4MHz crystal oscillator output, a DC/DC converter to generate 32V tuning voltage can be provided. Instead of RF modulator input, an antenna power supply input is possible.

The DTT 713XX has the possibility to activate an internal wide band RF AGC.

Tuning, band switching and internal RF AGC is controlled via I2C bus. The metal housing is in world standard tuner size. The module complies with the requirements of radiation, signal handling capability and immunity interference of CENELEC standards EN 55013 and EN 55020.



4. Pin Definitions

Pin	Symbol	Description
1	MOI	RF modulator input or antenna power supply input
2	RAG	RF AGC output / input
3	CAS	Chip I2C address select
4	SCL	I2C serial clock
5	SDA	I2C serial data
6	VC1	+5V supply voltage for loop through
7	VC2	+5V supply voltage for tuner
8	XTO/GPIO	4MHz crystal oscillator output or GPIO
9	VTs	Open or +3.3V
10	IF2	IF output symmetrical
11	IF1	IF output symmetrical

3. AUDIO AMPLIFIER STAGE WITH MP7722

3.1 General Description

The MP7722 is a stereo 20W Class D Audio amplifier, intended for use as low frequency power amplifier in a wide range of applications in radio and TV sets. It uses a minimum number of external components to complete a stereo Class D audio amplifier.

3.2 Features

- 2 x 20W Output at VDD = 24V into a 4Ω load
- THD+N = 0.06% at 1W, 8Ω
- 93% Efficiency at 20W
- Low Noise (190μV Typical)
- Switching Frequency Up to 1MHz
- 9.5V to 24V Operation from a Single Supply
- Integrated Startup and Shutdown Pop Elimination Circuit
- Thermal and Short Circuit Protection
- Integrated 180mΩ Switches
- Mute/Standby Modes (Sleep)
- Thermally Enhanced 20-Pin TSSOP Package with Exposed Pad

3.3 Applications

- Surround Sound DVD Systems
- Televisions
- Flat Panel Monitors
- Multimedia Computers
- Home Stereo Systems

3.4 Absolute Ratings

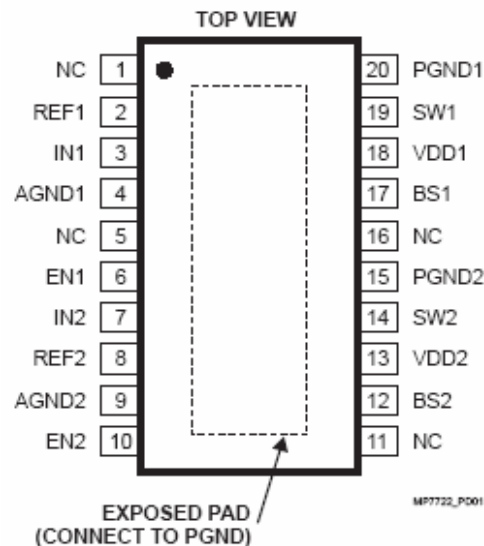
Supply Voltage V_{DD}	26V
BS Voltage	$V_{SW} - 0.3V$ to $V_{SW} + 6.5V$
Enable Voltage V_{EN}	-0.3V to +6V
V_{SW} , V_{PIN} , V_{NIN}	-1V to $V_{DD} + 1V$
AGND to PGND	-0.3V to +0.3V
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to +150°C

Recommended Operating Conditions ⁽²⁾

Supply Voltage V_{DD}	9.5V to 24V
Operating Temperature T_A	-40°C to +85°C

Thermal Resistance ⁽³⁾	θ_{JA}	θ_{JC}
TSSOP20F	40	6

3.5 Pinning



4. POWER STAGE

The DC voltages required at various parts of the chassis and inverters are provided by a main power supply unit and power interface board. The main power supply unit is designed for 24V and 12V DC supply. Power stage which is on-chassis generates +24V for audio amplifier, 1.8V and 3.3V stand by voltage and 8V, 12V, 5V and 3.3V supplies for other different parts of the chassis.

5. MICROCONTROLLER (VCTP)

5.1 General Features

The VCT 6wxyP is dedicated to high-quality FPD and double-scan TV sets. The VCT 6wxyP family is based on functional blocks contained and approved in existing products like VCT 49xxI, VSP 94x5B, and DPS 94xxA.

Each member of the family contains the entire audio, video, up-conversion processing for 4:3 and 16:9 50/

60 Hz progressive or 100/120 Hz interlaced stereo TV sets and the control/data interface for flat-panel displays. The integrated microcontroller is supported by a powerful OSD and graphics generator with integrated teletext acquisition.

Controller:

- High-performance 8-bit microcontroller, 8051 compatible
- Up to 512 kByte in system program Flash
- WST, PDC, VPS, and WSS acquisition
- Closed caption and V-chip acquisition
- Up to 10 page on chip teletext memory
- Up to 1000 pages with internal memory
- Up to 30 GPIO

Audio:

- Multistandard TV-sound demodulation:
 - All A2/NICAM standards
 - BTSC/SAP with DBX
 - EIA-J
- Baseband sound processing for loudspeaker channel:
 - Volume, bass, treble, loudness, balance
 - Spatial effect (e.g. pseudo stereo)
 - Micronas AROUND
(Virtual Dolby Surround optional)
 - Micronas BASS
 - BBE
 - SRS WOW
 - SRS TruSurround XT
 - Lipsync function

Video:

- CVBS, S-VHS, YCrCb and RGB inputs
- HDTV YPrPb and RGB inputs
- ITU656 input
- Linedoubling with vertical detail enhancement (without internal memory)
- State of the art motion adaptive up conversion (with internal memory)
- 4H adaptive comb filter for PAL/NTSC (without internal memory)
- 3D comb filter for PAL/NTSC (with internal memory) (Optional)
- Internal SDR RAM interface
- Powerful horizontal and vertical scaling inclusive
- Nonlinear horizontal scaling "panorama vision"
- picture adaptive image improvements (DCE, LSE, CTI, SCE, NCE)

- non-linear colorspace enhancement (NCE) with 32 programmable slopes and sections per RGB component (blue stretch, static black stretch, gamma correction).
- Dynamic contrast enhancement (DCE) (histogram based black stretch with peak black and activity detection and contrast adaption)
- Luma sharpness enhancement (LSE)
- Colour transient improvement (CTI)
- Selective colour enhancement (SCE) for skin tone correction, blue and green stretch

5.2 Multistandard Sound Processor (MSP) Features

The MSP receives the analog Sound IF signal from the tuner and converts it to digital with its internal SIF-AD converter. The MSP is able to demodulate all TV sound standards worldwide including the digital NICAM system. TV stereo sound standards that are unavailable for a specific **VCTP** version are processed in analog mono sound of the standard. In that case, stereo or bilingual processing will not be possible.

- Sound IF input
- Worldwide FM/AM-mono sound demodulation
- FM stereo sound demodulation (A2, EIA-J)
- BTSC/SAP demodulation with DBX
- NICAM demodulation
- FM radio & RDS/RBDS demodulation
- Automatic standard detection
- automatic volume correction (AVC)
- Automatic sound select
- Baseband processing for loudspeaker channel:
 - volume, bass, treble, loudness, balance
 - spatial effect (e.g. pseudo stereo)
 - Micronas AROUND
 - Micronas BASS
 - SRS WOW (optional)
 - SRS TruSurround XT (optional)
 - delayline for lipsync function (shared memory)
 - Virtual Dolby Surround (optional)
- 1 I2S input for external ATSC/DVD decoder
- 1 I2S interface for audio delayline
- 1 SPDIF output
- Audio i/o switches
 - 4 analog stereo line inputs and 2 analog stereo line outputs (configurable 5 analog stereo line inputs and 1 analog stereo line output)
 - 1 analog stereo loudspeaker output
 - 1 analog subwoofer output
 - 1 analog stereo headphone output

5.3 Video Features

The TVT is a Teletext decoder for decoding World System Teletext data, as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide-Screen Signalling (WSS) data used for PALplus transmissions (line 23). The device also supports Closed Caption acquisition and decoding.

The TVT provides an integrated general-purpose, fully 8051-compatible microcontroller with television-specific hardware features. The microcontroller has been enhanced to provide powerful features such as memory banking, data pointer, additional interrupts, shared memory access etc.

The TVT has an internal XRAM of 32 KB and a BOOT ROM of 4 KB. For operation the code is fetched from a 16bit FLASH, which can be addressed up to 1 MByte.

The controller with dedicated hardware does most of the internal TTX acquisition processing, transfers data to/from external memory interface, and receives/transmits data via I2C-bus interface. In combination with dedicated hardware, the slicer stores TTX data in a VBI buffer of 1 KB. The microcontroller firmware performs all the acquisition tasks (hamming and parity checks, page search, and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26 handling, FLOF/TOP and list-pages. The interface-to-user software is optimised for minimal overhead. TVT is realised in deep submicron technology with 1.8 V supply voltage and 3.3 V I/O (TTL compatible).

- 16 analog video inputs (4xCVBS/Y/C + 3xRGB/YCrCb/YPrPb)
- Video input switch matrix
- 3 analog video outputs (integrated Y+C adder)
- 24-bit RGB/H/V/clk input (e.g. ext. DVI decoder) or 656 8bit input
- 656 8bit input/output (e. g. for external high-end up conversion by FRCA)
- Multi-standard color decoder PAL/NTSC/SECAM including all substandards
- 2D adaptive comb filter for PAL/NTSC with vertical peaking
- 3D-comb filter for PAL/NTSC (Optional)
- Macrovision compliant multi-standard sync processing
- Trilevel sync slicer for HDTV
- Macrovision detection
- High-quality soft mixer controlled by Fast Blank (alpha blending)
- Fastblank monitor via I2C
- Noise measurement
- Letterbox detection (auto-wide)
- Split screen (OSD and video side by side) and AV PIP

5.4 Controller Features

The TVT is a Teletext decoder for decoding World System Teletext data, as well as Video Programming System (VPS), Program Delivery Control (PDC), and Wide-Screen Signalling (WSS) data used for PALplus transmissions (line 23). The device also supports Closed Caption acquisition and decoding.

The TVT provides an integrated general-purpose, fully 8051-compatible microcontroller with television-specific hardware features. The microcontroller has been enhanced to provide powerful features such as memory banking, data pointer, additional interrupts, shared memory access etc.

- High performance 8-bit microcontroller, 8051 instruction set compatible
- 81 MHz system clock, two machine cycles per instruction
- On-chip debug support (OCDS)
- Up to 512 kByte in system program Flash
- 256 byte on-chip program RAM
- 128 byte on-chip extended stack RAM

- 4-level, 24-input interrupt controller
- Patch module for 16 ROM locations
- Two 16-bit reloadable timers
- Capture compare timer for infrared decoding
- Watchdog timer
- Uart
- Real time clock
- PWM units (2 channels 14-bit, 6 channels 8-bit)
- 8-bit ADC (4 channels)
- I2C bus master/slave interface
- Up to 32 programmable I/O ports

5.5 OSD and Teletext Features

The on-chip display unit for displaying Level 1.5 Teletext data can also be used for customer-defined onscreen displays.

The TVT has an internal XRAM of 32 KB and a BOOT ROM of 4 KB. For operation the code is fetched from a 16bit FLASH, which can be addressed up to 1 MByte.

In combination with dedicated hardware, the slicer stores TTX data in a VBI buffer of 1 KB. The microcontroller firmware performs all the acquisition tasks (hamming and parity checks, page search, and evaluation of header control bits) once per field. Additionally, the firmware can provide high-end Teletext features like Packet-26 handling, FLOF/TOP and list-pages. The interface-to-user software is optimised for minimal overhead.

5.6 Port Allocation

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
1	656O6 P4_6 TDÖFW	IN/OUT	RtoGND	Digital 656 Bit 6 Output Port 4, Bit 6 Input/Output JTAG Interface Data Output (FW Controller)
2	656O5 P4_5 TDIFW	IN/OUT	RtoGND	Digital 656 Bit 5 Output Port 4, Bit 5 Input/Output JTAG Interface Data Input (FW Controller)
3	656O4 P4_4 TMSFW	IN/OUT	RtoGND	Digital 656 Bit 4 Output Port 4, Bit 4 Input/Output JTAG Interface Mode Select Input (FW Contr.)
4	656O3 P4_3 TCLK	IN/OUT	RtoSUP	Digital 656 Bit 3 Output Port 4, Bit 3 Input/Output JTAG Interface Clock Input (TV Controller)
5	656O2 P4_2 TDO	IN/OUT	RtoGND	Digital 656 Bit 2 Output Port 4, Bit 2 Input/Output JTAG Interface Data Output (TV Controller)

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
6	656O1 P4_1 TDI	IN/OUT	RtoGND	Digital 656 Bit 1 Output Port 4, Bit 1 Input/Output JTAG Interface Data Input (TV Controller)
7	656O0 P4_0 TMS	IN/OUT	RtoGND	Digital 656 Bit 0 Output (LSB) Port 4, Bit 0 Input/Output JTAG Interface Mode Select Input (TV Contr.)
8	RESETQ	IN/OUT	OBL	Reset Input/Output
9	AIN1R	IN	LV	Analog Audio 1 Input, Right
10	AIN1L	IN	LV	Analog Audio 1 Input, Left
11	AIN2R	IN	LV	Analog Audio 2 Input, Right
12	AIN2L	IN	LV	Analog Audio 2 Input, Left
13	AIN3R	IN	LV	Analog Audio 3 Input, Right
14	AIN3L	IN	LV	Analog Audio 3 Input, Left
15	AIN4R	IN	LV	Analog Audio 4 Input, Right
16	AIN4L	IN	LV	Analog Audio 4 Input, Left
17	VREFAU	ANA	OBL	Reference Voltage, Audio
18	VSUP8.0AU	SUPPLY	OBL	Supply Voltage Analog Audio, 8.0 V
19	GND A	SUPPLY	OBL	Ground Analog Audio, Platform Ground
20	SGND	ANA	OBL	Analog Signal GND
21	AOUT2R AIN5R	IN/OUT	LV	Analog Audio 2 Output, Right Analog Audio 5 Input, Right
22	AOUT2L AIN5L	IN/OUT	LV	Analog Audio 2 Output, Left Analog Audio 5 Input, Left
23	AOUT1R	OUT	LV	Analog Audio 1 Output, Right
24	AOUT1L	OUT	LV	Analog Audio 1 Output, Left
25	HEADPHONER	OUT	LV	Analog Headphone Output, Right
26	HEADPHONE L	OUT	LV	Analog Headphone Output, Left
27	SPEAKERR	OUT	LV	Analog Loudspeaker Output, Right
28	SPEAKERL	OUT	LV	Analog Loudspeaker Output, Left
29	SUBWOOFER TEST	IN/OUT	LV	Analog SUBWOOFER Output Test Input
30	VREFSIF	ANA	OBL	Reference Voltage, Audio SIF
31	SIFIN+	IN	GND	Differential Sound IF Input
32	SIFIN-	IN	GND	Differential Sound IF Input
33	VSUP5.0	SUPPLY	OBL	Supply Voltage Analog, 5.0 V

VCTP Pin No. PLQFP 208-1		Pin Name	Type	Connection (If not used)	Short Description
34		GND_A	SUPPLY	OBL	Ground Analog, Platform Ground
35		GND3.3DIG	SUPPLY	OBL	Ground Digital Interfaces
36		VSUP3.3DIG	SUPPLY	OBL	Supply Voltage Digital Interfaces, 3.3 V
37		SPDIF_OUT	OUT	LV	SPDIF Output
38		I2S_DA_IN	IN	GND	Audio Bus Data Input
39		I2S_CL	IN	GND	Audio Bus Clock Input
40		I2S_WS	IN	GND	Audio Bus Word Strobe Input
41		I2S_DEL_OUT	OUT/IN	LV	Audio Delay Line Bus Data Output/Input
42		I2S_DEL_IN	IN/OUT	GND	Audio Delay Line Bus Data Input/Output
43		I2S_DEL_CL	OUT/IN	LV	Audio Delay Line Bus Clock Output/Input
44		I2S_DEL_WS	OUT/IN	LV	Audio Delay Line Word Strobe Output/Input
45		VSUP3.3RAM	SUPPLY	OBL	Supply Voltage Ram, 3.3 V
46		GND3.3RAM	SUPPLY	OBL	Ground Ram
47		DVS	IN	GND	Digital or Analog Video VSYNC HD Input
48		DEN	IN	GND	Digital Video Enable Input
49		DCLK	IN	GND	Digital Video Clock Input
50		DRI7	IN	GND	Digital Video Red 7 Input
51		DRI6	IN	GND	Digital Video Red 6 Input
52		DRI5	IN	GND	Digital Video Red 5 Input
53		DRI4	IN	GND	Digital Video Red 4 Input
54		DRI3	IN	GND	Digital Video Red 3 Input
55		DRI2	IN	GND	Digital Video Red 2 Input
56		DRI1	IN	GND	Digital Video Red 1 Input
57		DRI0	IN	GND	Digital Video Red 0 Input (LSB)
58		DGI7	IN	GND	Digital Video Green 7 Input
59		DGI6	IN	GND	Digital Video Green 6 Input
60		DGI5	IN	GND	Digital Video Green 5 Input
61		DGI4	IN	GND	Digital Video Green 4 Input
62		DGI3	IN	GND	Digital Video Green 3 Input
63		DGI2	IN	GND	Digital Video Green 2 Input
64		DGI1	IN	GND	Digital Video Green 1 Input

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
65	DGI0	IN	GND	Digital Video Green 0 Input (LSB)
66	DBI7	IN	GND	Digital Video Blue 7 Input
67	DBI6	IN	GND	Digital Video Blue 6 Input
68	DBI5	IN	GND	Digital Video Blue 5 Input
69	DBI4	IN	GND	Digital Video Blue 4 Input
70	DBI3	IN	GND	Digital Video Blue 3 Input
71	DBI2	IN	GND	Digital Video Blue 2 Input
72	DBI1	IN	GND	Digital Video Blue 1 Input
73	DBI0	IN	GND	Digital Video Blue 0 Input (LSB)
74	GND3.3DRI	SUPPLY	OBL	Ground Digital Ram Interface
75	VSUP3.3DRI	SUPPLY	OBL	Supply Voltage Digital Ram Interface, 3.3 V
76	GND3.3COM	SUPPLY	OBL	Ground Common
77	VSUP3.3COM	SUPPLY	OBL	Supply Voltage Common, 3.3V
78	XTALIN	IN	OBL	Analog Crystal Input
79	XTALOUT	OUT	OBL	Analog Crystal Output
80	CLKOUT	OUT	RtoGND	Digital 20MHz Clock Output
81	VSO	OUT	RtoGND	Vertical Sync Output, Frontend
82	HSO	OUT	RtoGND	Horizontal Sync Output, Frontend
83	SCL	IN/OUT	OBL	I ² C Bus Clock Input/Output
84	SDA	IN/OUT	OBL	I ² C Bus Data Input/Output
85	GND3.3FL	SUPPLY	OBL	Ground Flash
86	VSUP3.3FL	SUPPLY	OBL	Supply Voltage Flash, 3.3 V
87	P2_0	IN/OUT	RtoGND	Port 2, Bit 0 Input/Output
88	P2_1	IN/OUT	RtoGND	Port 2, Bit 1 Input/Output
89	P2_2	IN/OUT	RtoGND	Port 2, Bit 2 Input/Output
90	P2_3	IN/OUT	RtoGND	Port 2, Bit 3 Input/Output
91	P2_4 TDI	IN/OUT	RtoGND	Port 2, Bit 4 Input/Output JTAG Interface Data Input
92	P2_5 TMS	IN/OUT	RtoGND	Port 2, Bit 5 Input/Output JTAG Interface Mode Select Input
93	OSDV DBO2_0	IN/OUT	RtoGND	Graphic Vertical Sync Input/Output Channel 2 Digital 0 Blue Output (LSB)

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
94	OSDH DBO2_1	IN/OUT	RtoGND	Graphic Horizontal Sync Input/Output Channel 2 Digital 1 Blue Output
95	GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
96	VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
97	OSDCLK DBO2_2	IN/OUT	RtoGND	Graphic Clock Input/Output Channel 2 Digital 2 Blue Output
98	OSDFSW DBO2_3	IN/OUT	RtoGND	Graphic Fast Switch Input/Output Channel 2 Digital 3 Blue Output
99	OSDHCS1 P3_6 DBO2_4	IN/OUT	RtoGND	Graphic Half Contrast 1 Input/Output Port 3, Bit 6 Input/Output Channel 2 Digital 4 Blue Output
100	OSDHCS0 P3_7 DBO2_5	IN/OUT	RtoGND	Graphic Half Contrast 0 Input/Output (LSB) Port 3, Bit 7 Input/Output Channel 2 Digital 5 Blue Output
101	OSDB3 P3_5 DBO2_6	IN/OUT	RtoGND	Graphic Blue 3 Input/Output (MSB) Port 3, Bit 5 Input/Output Channel 2 Digital 6 Blue Output
102	OSDB2 P3_4 DBO2_7	IN/OUT	RtoGND	Graphic Blue 2 Input/Output Port 3, Bit 4 Input/Output Channel 2 Digital 7 Blue Output (MSB)
103	OSDB1 DGO2_0	IN/OUT	RtoGND	Graphic Blue 1 Input/Output Channel 2 Digital 0 Green Output (LSB)
104	OSDB0 DGO2_1	IN/OUT	RtoGND	Graphic Blue 0 Input/Output Channel 2 Digital 1 Green Output
105	OSDG3 P3_3 DGO2_2	IN/OUT	RtoGND	Graphic Green 3 Input/Output (MSB) Port 3, Bit 3 Input/Output Channel 2 Digital 2 Green Output
106	OSDG2 P3_2 DGO2_3	IN/OUT	RtoGND	Graphic Green 2 Input/Output Port 3, Bit 2 Input/Output Channel 2 Digital 3 Green Output
107	OSDG1 DGO2_4	IN/OUT	RtoGND	Graphic Green 1 Input/Output Channel 2 Digital 4 Green Output
108	OSDG0 DGO2_5	IN/OUT	RtoGND	Graphic Green 0 Input/Output Channel 2 Digital 5 Green Output
109	OSDR3 P3_1 DGO2_6	IN/OUT	RtoGND	Graphic Red 3 Input/Output (MSB) Port 3, Bit 1 Input/Output Channel 2 Digital 6 Green Output
110	OSDR2 P3_0 DGO2_7	IN/OUT	RtoGND	Graphic Red 2 Input/Output Port 3, Bit 0 Input/Output Channel 2 Digital 7 Green Output (MSB)
111	OSDR1 DRO2_0	IN/OUT	RtoGND	Graphic Red 1 Input/Output Channel 2 Digital 0 Red Output (LSB)

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
112	OSDR0 DRO2_1	IN/OUT	RtoGND	Graphic Red 0 Input/Output (LSB) Channel 2 Digital 1 Red Output
113	GND3.3IO1	SUPPLY	OBL	Ground Digital Input/Output Port 1
114	VSUP3.3IO1	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
115	PCS5 P2_7	IN/OUT	RtoGND	Flat Panel Control Select 5 Output Port 2, Bit 7 Input/Output
116	PCS4 P2_6	IN/OUT	RtoGND	Flat Panel Control Select 4 Output Port 2, Bit 6 Input/Output
117	PCS3 P4_1	IN/OUT	RtoGND	Flat Panel Control Select 3 DE2 Output Port 4, Bit 1 Input/Output
118	PCS2 P4_0	IN/OUT	RtoGND	Flat Panel Control Select 2 DE1 Output Port 4, Bit 0 Input/Output
119	PCS1 P4_3	IN/OUT	RtoGND	Flat Panel Control Select 1 H Output Port 4, Bit 3 Input/Output
120	PCS0 P4_2	IN/OUT	RtoGND	Flat Panel Control Select 0 V Output Port 4, Bit 2 Input/Output
121	PCLK2	OUT	LV	Flat Panel Control Clock 2 Output
122	PCLK1	OUT	LV	Flat Panel Control Clock 1 Output
123	GND1.8DIG	SUPPLY	OBL	Ground Digital Core
124	VSUP1.8DIG	SUPPLY	OBL	Supply Voltage Digital Core, 1.8 V
125	DBO1_0 DRO2_2 LVDSA_4P	OUT	LV	Channel 1 Digital 0 Blue Output ¹⁾ (LSB) Channel 2 Digital 2 Red Output ¹⁾ LVDS Channel 1 bit 4 Positive Output ²⁾
126	DBO1_1 DRO2_3 LVDSA_4N	OUT	LV	Channel 1 Digital 1 Blue Output ¹⁾ Channel 2 Digital 3 Red Output ¹⁾ LVDS Channel 1 bit 4 Negative Output ²⁾
127	DBO1_2 DRO2_4 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Blue Output ¹⁾ Channel 2 Digital 4 Red Output ¹⁾ Supply Digital Voltage LVDS ²⁾ Port, 3.3 V
128	DBO1_3 DRO2_5 LVDSA_3P	OUT	LV	Channel 1 Digital 3 Blue Output ¹⁾ Channel 2 Digital 5 Red Output ¹⁾ LVDS Channel 1 bit 3 Positive Output ²⁾
129	DBO1_4 DRO2_6 LVDSA_3N	OUT	LV	Channel 1 Digital 4 Blue Output ¹⁾ Channel 2 Digital 6 Red Output ¹⁾ LVDS Channel 1 bit 3 Negative Output ²⁾
130	DBO1_5 DRO2_7 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Blue Output ¹⁾ Channel 2 Digital 7 Red Output ¹⁾ (MSB) Ground Digital LVDS ²⁾ , 3.3 V
131	DBO1_6 DBO1_0 LVDSA_CLKP	OUT	LV	Channel 1 Digital 6 Blue Output ¹⁾ Channel 1 Digital 0 Blue Output ¹⁾ (LSB) LVDS Channel 1 Clock Positive Output ²⁾

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
132	DBO1_7 DBO1_1 LVDSA_CLKN	OUT	LV	Channel 1 Digital 7 Blue Output ¹⁾ Channel 1 Digital 1 Blue Output ¹⁾ LVDS Channel 1 Clock Negative Output ²⁾
133	VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Digital Output ¹⁾ Port 2 Supply Digital Voltage LVDS ²⁾ , 3.3 V
134	GND3.3IO2 LVDSA_2P	SUPPLY OUT	OBL LV	Ground Voltage Output ¹⁾ Port 2, 3.3 V LVDS Channel 1 bit 2 Positive Output ²⁾
135	DBO1_8 DBO1_2 LVDSA_2N	OUT	LV	Channel 1 Digital 8 Blue Output ¹⁾ Channel 1 Digital 2 Blue Output ¹⁾ LVDS Channel 1 bit 2 Negative Output ²⁾
136	DBO1_9 DBO1_3 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 9 Blue Output ¹⁾ (MSB) Channel 1 Digital 3 Blue Output ¹⁾ Ground Digital LVDS ²⁾ , 3.3 V
137	DGO1_0 DBO1_4 LVDSA_1P	OUT	LV	Channel 1 Digital 0 Green Output ¹⁾ (LSB) Channel 1 Digital 4 Blue Output ¹⁾ LVDS Channel 1 bit 1 Positive Output ²⁾
138	DGO1_1 DBO1_5 LVDSA_1N	OUT	LV	Channel 1 Digital 1 Green Output ¹⁾ Channel 1 Digital 5 Blue Output ¹⁾ LVDS Channel 1 bit 1 Negative Output ²⁾
139	DGO1_2 DBO1_6 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 2 Green Output ¹⁾ Channel 1 Digital 6 Blue Output ¹⁾ Supply Digital Voltage LVDS ²⁾ , 3.3 V
140	DGO1_3 DBO1_7 LVDSA_0P	OUT	LV	Channel 1 Digital 3 Green Output ¹⁾ Channel 1 Digital 7 Blue Output ¹⁾ (MSB) LVDS Channel 1 bit 0 Positive Output ²⁾
141	DGO1_4 DGO1_0 LVDSA_0N	OUT	LV	Channel 1 Digital 4 Green Output ¹⁾ Channel 1 Digital 0 Green Output ¹⁾ (LSB) LVDS Channel 1 bit 0 Negative Output ²⁾
142	DGO1_5 DGO1_1 VSUP1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 5 Green Output ¹⁾ Channel 1 Digital 1 Green Output ¹⁾ Supply Analog Voltage LVDS ²⁾ , 1.8 V
143	DGO1_6 DGO1_2 REXT	OUT ANA	LV OBL	Channel 1 Digital 6 Green Output ¹⁾ Channel 1 Digital 2 Green Output ¹⁾ LVDS External Resistor ²⁾
144	DGO1_7 DGO1_3 GND1.8LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Green Output ¹⁾ Channel 1 Digital 3 Green Output ¹⁾ Ground Analog LVDS ²⁾ , 1.8 V
145	DGO1_8 DGO1_4 LVDSB_3P	OUT	LV	Channel 1 Digital 8 Green Output ¹⁾ Channel 1 Digital 4 Green Output ¹⁾ Dual-LVDS Channel 2 bit 3 Positive Output ²⁾
146	DGO1_9 DGO1_5 LVDSB_3N	OUT	LV	Channel 1 Digital 9 Green Output ¹⁾ (MSB) Channel 1 Digital 5 Green Output ¹⁾ Dual-LVDS Channel 2 bit 3 Negative Output ²⁾

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
147	DRO1_0 DGO1_6 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 0 Red Output ¹⁾ (LSB) Channel 1 Digital 6 Green Output ¹⁾ Ground Digital LVDS ²⁾ , 3.3 V
148	DRO1_1 DGO1_7 LVDSBCLKP	OUT	LV	Channel 1 Digital 1 Red Output ¹⁾ Channel 1 Digital 7 Green Output ¹⁾ (MSB) Dual-LVDS Channel 2 Clock Positive Output ²⁾
149	GND3.3IO2 LVDSBCLKN	SUPPLY OUT	OBL LV	Ground Digital Output ¹⁾ Port 2 Dual-LVDS Channel 2 Clock Negative Output ²⁾
150	VSUP3.3IO2 VSUP3.3LVDS	SUPPLY	OBL	Supply Voltage Output ¹⁾ Port 2, 3.3 V Supply Digital Voltage LVDS ²⁾ , 3.3 V
151	DRO1_2 DRO1_0 LVDSB_2P	OUT	LV	Channel 1 Digital 2 Red Output ¹⁾ Channel 1 Digital 0 Red Output ¹⁾ (LSB) Dual-LVDS Channel 2 bit 2 Positive Output ²⁾
152	DRO1_3 DRO1_1 LVDSB_2N	OUT	LV	Channel 1 Digital 3 Red Output ¹⁾ Channel 1 Digital 1 Red Output ¹⁾ Dual-LVDS Channel 2 bit 2 Negative Output ²⁾
153	DRO1_4 DRO1_2 GND3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 4 Red Output ¹⁾ Channel 1 Digital 2 Red Output ¹⁾ Ground Digital LVDS ²⁾ , 3.3 V
154	DRO1_5 DRO1_3 LVDSB_1P	OUT	LV	Channel 1 Digital 5 Red Output ¹⁾ Channel 1 Digital 3 Red Output ¹⁾ Dual-LVDS Channel 2 bit 1 Positive Output ²⁾
155	DRO1_6 DRO1_4 LVDSB_1N	OUT	LV	Channel 1 Digital 6 Red Output ¹⁾ Channel 1 Digital 4 Red Output ¹⁾ Dual-LVDS Channel 2 bit 1 Negative Output ²⁾
156	DRO1_7 DRO1_5 VSUP3.3LVDS	OUT SUPPLY	LV OBL	Channel 1 Digital 7 Red Output ¹⁾ Channel 1 Digital 5 Red Output ¹⁾ Supply Digital Voltage LVDS ²⁾ , 3.3 V
157	DRO1_8 DRO1_6 LVDSB_0P	OUT	LV	Channel 1 Digital 8 Red Output ¹⁾ Channel 1 Digital 6 Red Output ¹⁾ Dual-LVDS Channel 2 bit 0 Positive Output ²⁾
158	DRO1_9 DRO1_7 LVDSB_0N	OUT	LV	Channel 1 Digital 9 Red Output ¹⁾ (MSB) Channel 1 Digital 7 Red Output ¹⁾ (MSB) Dual-LVDS Channel 2 bit 0 Negative Output ²⁾
159	P1_7 TDO	IN/OUT	RtoGND	Port 1, Bit 7 Input/Output JTAG Interface Data Output
160	P1_6 TCLK	IN/OUT	RtoSUP	Port 1, Bit 6 Input/Output JTAG Interface Clock Input
161	P1_5	IN/OUT	RtoGND	Port 1, Bit 5 Input/Output
162	P1_4	IN/OUT	RtoGND	Port 1, Bit 4 Input/Output
163	GND3.3DAC	SUPPLY	OBL	Ground DAC
164	VSUP3.3DAC	SUPPLY	OBL	Supply Voltage DAC, 3.3V

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
165	P1_3 ROUT PWM3	IN/OUT	RtoGND	Port 1, Bit 3 Input/Output Analog Red Output PWM Bit 3 Output
166	P1_2 GOUT PWM2	IN/OUT	RtoGND	Port 1, Bit 2 Input/Output Analog Green Output PWM Bit 2 Output
167	P1_1 BOUT PWM1	IN/OUT	RtoGND	Port 1, Bit 1 Input/Output Analog Blue Output PWM Bit 1 Output
168	P1_0 SVMOUT REV	IN/OUT	RtoGND	Port 1, Bit 0 Input/Output Scan Velocity Modulation Output REV Output
169	VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
170	VSUP3.3FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 3.3 V
171	VIN22 DHS	IN	LV	Analog Video 22 H-Sync Input Digital Video H-Sync Input
172	VIN21	IN	LV	Analog Video 21 B HD Input
173	VIN20	IN	LV	Analog Video 20 G HD Input
174	VIN19	IN	LV	Analog Video 19 R HD Input
175	VIN18	IN	LV	Analog Video 18 Fast Blank 2 Input
176	VIN17	IN	LV	Analog Video 17 B HD Input
177	VIN16	IN	LV	Analog Video 16 G HD Input
178	VIN15	IN	LV	Analog Video 15 R HD Input
179	VIN13	IN	LV	Analog Video 13 B HD Input
180	VIN12	IN	LV	Analog Video 12 G HD Input
181	VIN11	IN	LV	Analog Video 11 R HD Input
182	VIN9	IN	LV	Analog Video 9 Y or B SD Input
183	VIN8	IN	LV	Analog Video 8 C or Fast Blank 1 Input
184	VIN7	IN	LV	Analog Video 7 Y or G SD Input
185	VSUP1.8FE	SUPPLY	OBL	Supply Voltage Analog Video Frontend, 1.8 V
186	GND A	SUPPLY	OBL	Analog Video Frontend, Platform Ground
187	VIN6	IN	LV	Analog Video 6 C or R SD Input
188	VIN5	IN	LV	Analog Video 5 Y/CVBS Input
189	VIN3	IN	LV	Analog Video 3 CVBS Input
190	VIN2	IN	LV	Analog Video 2 CVBS Input

VCTP Pin No. PLQFP 208-1	Pin Name	Type	Connection (If not used)	Short Description
191	VIN1	IN	LV	Analog Video 1 CVBS Input
192	VSUP3.3VO	SUPPLY	OBL	Supply Voltage Analog Video Output, 3.3 V
193	VOU3	OUT	LV	Analog CVBS Video 3 Output
194	VOU2	OUT	LV	Analog CVBS Video 2 Output
195	VOU1	OUT	LV	Analog CVBS Video 1 Output
196	GND3.3IO3	SUPPLY	OBL	Ground Digital Input/Output Port 1
197	VSUP3.3IO3	SUPPLY	OBL	Supply Voltage Input/Output Port 1, 3.3 V
198	656I0 P3_0	IN/OUT	RtoGND	Digital 656 Bit 0 Input (LSB) Port 3, Bit 0 Input/Output
199	656I1 P3_1	IN/OUT	RtoGND	Digital 656 Bit 1 Input Port 3, Bit 1 Input/Output
200	656I2 P3_2	IN/OUT	RtoGND	Digital 656 Bit 2 Input Port 3, Bit 2 Input/Output
201	656I3 P3_3	IN/OUT	RtoGND	Digital 656 Bit 3 Input Port 3, Bit 3 Input/Output
202	656I4 P3_4	IN/OUT	RtoGND	Digital 656 Bit 4 Input Port 3, Bit 4 Input/Output
203	656I5 P3_5	IN/OUT	RtoGND	Digital 656 Bit 5 Input Port 3, Bit 5 Input/Output
204	656I6 P3_6	IN/OUT	RtoGND	Digital 656 Bit 6 Input Port 3, Bit 6 Input/Output
205	656I7 P3_7	IN/OUT	RtoGND	Digital 656 Bit 7 Input Port 3, Bit 7 Input/Output
206	656CLKI	IN	GND	Digital 656 Clock Input
207	656CLKO	OUT	LV	Digital 656 Clock Output
208	656O7 P4_7 TCLKFW	IN/OUT	RtoSUP	Digital 656 Bit 7 Output Port 4, Bit 7 Input/Output JTAG Interface Clock Input (FW Controller)
¹⁾ TTL output version only ²⁾ LVDS output version only				

6. DRX 3961A

6.1 General Description

The DSP-based Analog TV IF Demodulator DRX 396xA performs the entire multistandard Quasi Split Sound (QSS) TV IF processing, AGC, video demodulation, and generation of the sound IF (SIF), requiring only one SAW filter. The IC is designed for applications in TV sets, VCRs, PC cards, and TV tuners.

The alignment-free DRX 396xA does not need special external components. All control functions and status registers are accessible via I2C bus interface.

6.2 Features

- Multistandard QSS IF processing with a single SAW
- Highly reduced amount of external components (no tank circuit, no potentiometers, no SAW switching)

- Programmable IF frequency (38.9 MHz, 45.75 MHz, 32.9 MHz, 58.75 MHz, 36.125 MHz etc.)
- Digital IF processing for the following standards: B/G, D/K, I, L/L', and M/N
- Standard specific digital post filtering
- Standard specific digital video/audio splitting
- Standard specific digital picture carrier recovery:
 - Alignment-free
 - Quartz-stable and accurate
 - Stable frequency lock at 100% modulation and overmodulation up to 150%
 - Quartz-accurate AFC information
- Programmable standard specific digital group delay equalization
- Automatically frequency-adjusted Nyquist slope, therefore optimum picture and sound performance over complete lock in frequency range
- Standard-specific digital AGC and delayed tuner AGC with programmable tuner take-over point
- Fast AGC due to linear structure
- Adaptive back porch control, therefore fast positive modulation AGC
- No sound traps needed at video output
- SIF output with standard-dependent pre-filtering and amplitude-controlled output level
- Optimal sound SNR due to carrier recovery without quadrature distortions
- FM radio capability without external components and with standard TV tuner
- Prepared for digital TV (DVB-C, DVB-T, ATSC)
- I2C bus interface

7. SERIAL 64K I2C EEPROM M24C64WBN6

7.1 General Description

M24C64WBN6 is a 64 Kbit Electrically Erasable PROM. These I2C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192x8 bits. It supports 400kHz Protocol I2C uses a two-wire serial interface, comprising a bi-directional data line and a clock line.

The M24C64WBN6 is available in the standard 8-pin (Vcc, WC, SDA (I2C data), SCL (I2C clock), Vss, E0, E1, E2). WC pin is critical pin. If WP is high, writing is not possible to EEPROM. If WP is low, writing is possible to EEPROM.

7.2 Features

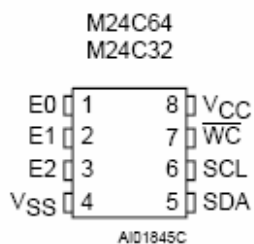
- Two-Wire I2C Serial Interface Supports 400kHz Protocol
- Single Supply Voltage:
 - 4.5 to 5.5V for M24Cxx
 - 2.5 to 5.5V for M24Cxx-W
 - 1.8 to 5.5V for M24Cxx-R
- Write Control Input
- BYTE and PAGE WRITE (up to 32 Bytes)

- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- More than 1 Million Erase/Write Cycles
- More than 40-Year Data Retention

7.3 Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
T _{STG}	Storage Temperature	−65	150	°C
T _{LEAD}	Lead Temperature during Soldering	See note ¹		°C
V _{IO}	Input or Output range	−0.50	6.5	V
V _{CC}	Supply Voltage	−0.50	6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ²	−4000	4000	V

7.4 Pinning



E0, E1, E2	Chip Enable
SDA	Serial Data
SCL	Serial Clock
\overline{WC}	Write Control
V _{CC}	Supply Voltage
V _{SS}	Ground

8. CLASS AB STEREO HEADPHONE DRIVER TDA1308

8.1. General Description

The TDA1308 is an integrated class AB stereo headphone driver contained in an SO8 or a DIP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications. It gets its input from two analog audio outputs (DACA_L and DACA_R) of MSP 34x0G. The gain of the output is adjustable by the feedback resistor between the inputs and outputs.

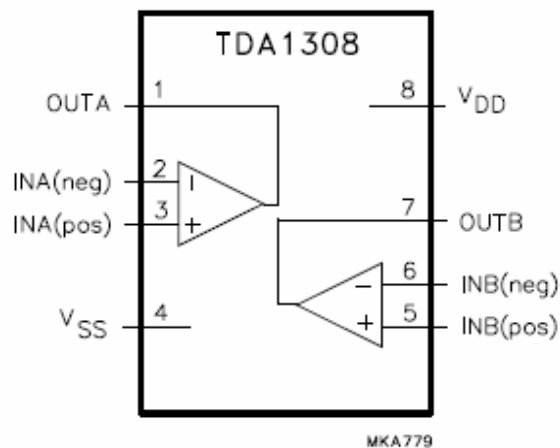
8.2 Features

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
- High signal-to-noise ratio

- High slew rate
- Low distortion
- Large output voltage swing.
- Power supply maximum 60 mW to 32Ω (THD<0.1%)
- 5V single supply
- SNR 110 dB
- Power supply ripple rejection
- Typically 3 mA supply current at no load

8.3. Pinning

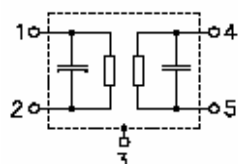
SYMBOL	PIN	DESCRIPTION
OUTA	1	Output A
INA(neg)	2	Inverting input A
INA(pos)	3	Non-inverting input A
V _{SS}	4	Negative supply
INB(pos)	5	Non-inverting input B
INB(neg)	6	Inverting input B
OUTB	7	Output B
V _{DD}	8	Positive supply



9. SAW FILTER X6966M

9.1 Features:

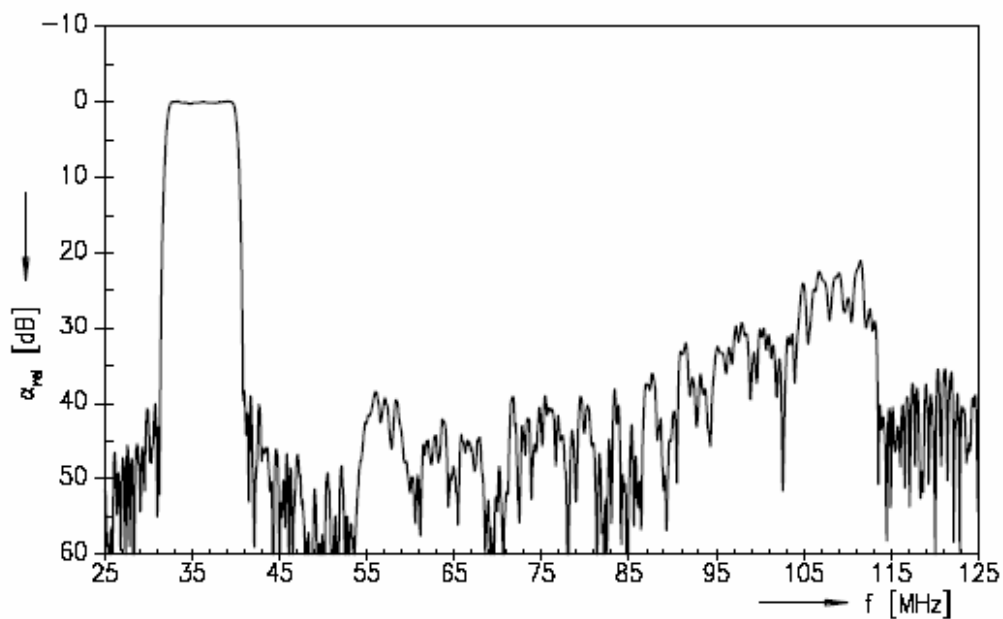
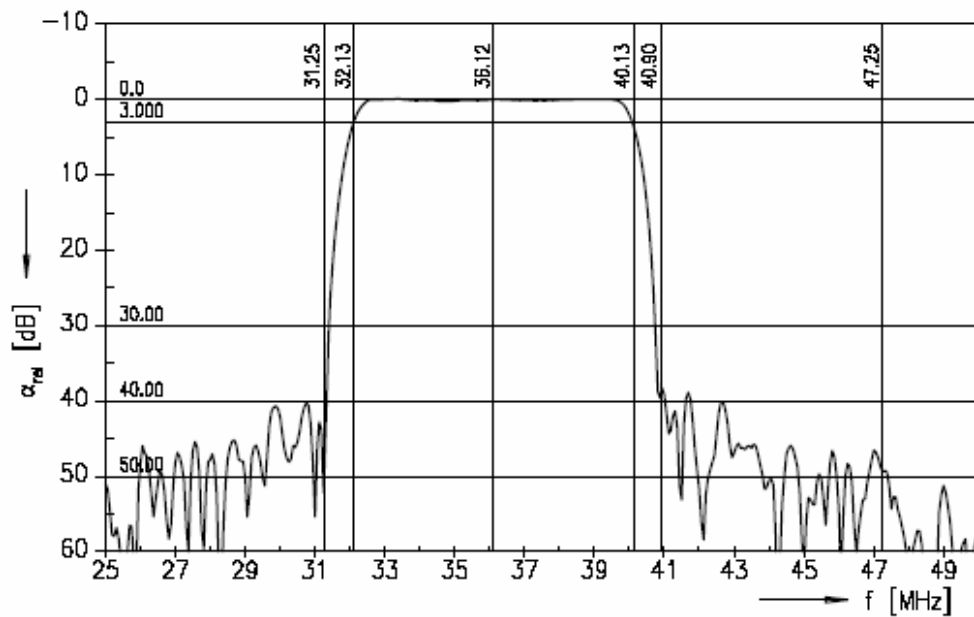
- IF filter for digital cable TV
- Plastic package SIP5K



9.2 Pin configuration:

- 1 Input
- 2 Input - ground
- 3 Chip carrier - ground
- 4 Output
- 5 Output

9.3 Frequency response:



10. IC DESCRIPTIONS AND INTERNAL BLOCK DIAGRAM

LM1117
LM1086
MP1593
FDC642P
SIL9011
24LC02
 μ PA672T
M74HC4052
Max809
24LC21

10.1. LM1117

10.1.1. General Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within $\pm 1\%$. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10 μ F tantalum capacitor is required at the output to improve the transient response and stability.

10.1.2. Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range
- LM1117 0°C to 125°C
- LM1117I -40°C to 125°C

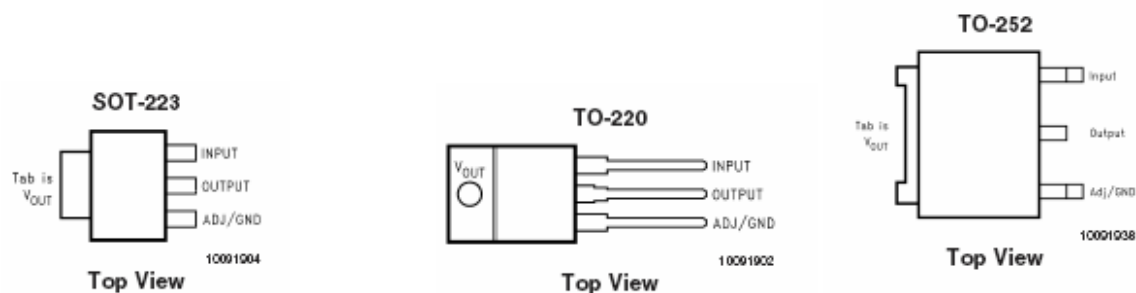
10.1.3. Applications

- 2.85V Model for SCSI-2 Active Termination
- Post Regulator for Switching DC/DC Converter
- High Efficiency Linear Regulators 15
- 32" TFT TV Service Manual
- Battery Charger
- Battery Powered Instrumentation

10.1.4. Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
DC Input Voltage	V_{IN}		7	V
Lead Temperature (Soldering, 5 Seconds)	T_{SOL}		260	°C
Storage Temperature Range	T_{STG}	-65	150	°C
Operating Junction Temperature Range	T_{OPR}	0	125	°C

10.1.5. Pinning



10.2. LM1086

10.2.1. General Description

The LM1086 is a low dropout three terminal regulator with 1.5A output current capability. The output voltage is adjustable with the use of a resistor divider. Dropout is guaranteed at a maximum of 500 mV at maximum output current. Its low dropout voltage and fast transient response make it ideal for low voltage microprocessor applications. Internal current and thermal limiting provides protection against any overload condition that would create excessive junction temperature.

10.2.2. Features

- Low Dropout Voltage 500mV at 1.5A Output Current
- Fast Transient Response
- 0.015% Line Regulation
- 0.1% Load Regulation
- Current Limiting and Thermal Protection.
- Adjustable or Fixed Output Voltage(1.8, 2.5, 2.85, 3.0, 3.3, 3.45, 5.0V)
- Surface Mount Package SOT-223 & TO-263 (D2 Package)
- 100% Thermal Limit Burn-in

10.2.3. Applications

- Battery Charger
- Adjustable Power Supplies
- Constant Current Regulators
- Portable Instrumentation
- High Efficiency Linear Power Supplies

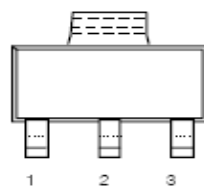
- High Efficiency "Green" Computer Systems
- SMPS Post-Regulator
- Power PC Supplies
- Powering VGA & Sound Card

10.2.4. Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	VALUE	UNIT
Supply Voltage	V _{in}	7	V
Operating Junction Temperature Range	T _{opr}	0–125	°C
Storage Temperature Range	T _{stg}	–65–150	°C
Thermal Resistance Junction to Case TO-263	T _{jc}	3	C/W
Thermal Resistance Junction to Ambient TO-263	T _{ja}	60	C/W
Lead Temperature (Soldering) 10 sec.	T _{sol}	300	°C
Maximum Output Current	I _{max}	1.5	A

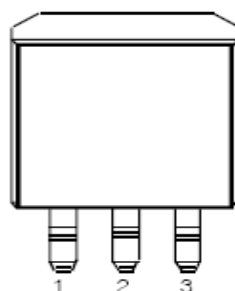
10.2.5. Pinning

SOT-223 PKG (FRONT VIEW)



PIN FUNCTION
 1. Adj/Gnd
 2. Vout
 3. Vin

TO-263 (D2 PKG, FRONT VIEW)



PIN FUNCTION
 1. Adj/Gnd
 2. Vout
 3. Vin

10.3. MP1593

10.3.1. General Description

The MP1593 is a step-down regulator with an internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilisation. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20µA of supply current. The MP1593 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

10.3.2. Features

- 3A Output Current
- Programmable Soft-Start
- 100mΩ Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20μA Shutdown Mode
- Fixed 385KHz Frequency
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 28V Operating Input Range
- Output Adjustable from 1.22V
- Under Voltage Lockout
- Available in 8-Pin SOIC Package

10.3.3. Applications

- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- Flat Panel TVs
- Set-Top Boxes
- Cigarette Lighter Powered Devices
- DVD/PVR Devices

10.3.4. Absolute Maximum Ratings

Supply Voltage V_{IN}	-0.3V to 30V
Switch Voltage V_{SW}	-0.5V to $V_{IN}+0.3V$
Boost Voltage V_{BS}	$V_{SW}-0.3V$ to $V_{SW}+6V$
All Other Pins.....	-0.3V to 6V
Junction Temperature.....	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C

10.3.5. Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		$V_{EN} = 0V$		20	30	μA
Supply Current		$V_{EN} = 2.6V$; $V_{FB} = 1.4V$		1.0	1.2	mA
Feedback Voltage	V_{FB}	$4.75V \leq V_{IN} \leq 28V$; $V_{COMP} < 2V$	1.194	1.222	1.250	V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	$\Delta I_{COMP} = \pm 10 \mu A$	500	800	1120	$\mu A/V$
High Side Switch On Resistance	$R_{DS(ON)1}$			100	140	m Ω
Low Side Switch On Resistance	$R_{DS(ON)2}$			10		Ω
High Side Switch Leakage Current		$V_{EN} = 0V$; $V_{SW} = 0V$		0	10	μA
Current Limit			3.3	4.7	6.5	A
Current Sense to COMP Transconductance	G_{CS}			6.2		A/V
Oscillation Frequency	f_{OSC1}		335	385	435	KHz
Short Circuit Oscillation Frequency	f_{OSC2}	$V_{FB} = 0V$	25	45	60	KHz
Maximum Duty Cycle	D_{MAX}	$V_{FB} = 1.0V$		90		%
Minimum Duty Cycle	D_{MIN}	$V_{FB} = 1.5V$			0	%
EN Threshold Voltage			0.9	1.2	1.5	V

10.3.6. Pinning

Pin1:BS

High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capacitor from SW to BS to power the high side switch.

Pin2:IN

Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 28V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC.

Pin3:SW

Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.

Pin4:GND

Ground.

Pin5:FB

Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 1.222V.

Pin6:COMP

Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.

Pin7:EN

Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive EN low to turn it off. An Under Voltage Lockout (UVLO) function can be implemented by the addition of a resistor divider from VIN to GND. For complete low current shutdown its needs to be less than 0.7V. For automatic startup, leave EN unconnected.

Pin8:SS

Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 10ms. To disable the soft-start feature, leave SS unconnected.

10.4. FDC642P

10.4.1. General Description

This p-channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench process that has been especially tailored to minimize on state resistance and yet maintain low gate charge for superior switching performance.

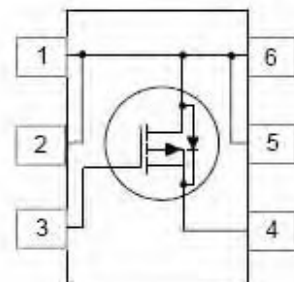
10.4.2 . Features

- -4 A, -20 V. $R_{DS(ON)} = 0.065 \Omega @ V_{GS} = -4.5 V$
 $R_{DS(ON)} = 0.100 \Omega @ V_{GS} = -2.5 V$
- Fast switching speed.
- Low gate charge (7.2nC typical).
- High performance trench technology for extremely low $R_{DS(ON)}$.
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1mm thick).

10.4.3. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	-20	V
V_{GS}	Gate-Source Voltage	±8	V
I_D	Drain Current - Continuous (Note 1)	-4	A
	Drain Current - Pulsed (Note 1a)	-20	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.6	W
		0.8	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

10.4.4. Pinning



10.5. SIL9011

The Sil 9011 is a third generation HDMI receiver compatible with the HDMI 1.1 specification. Backwards compatibility with DVI 1.0 allows HDMI systems to connect to existing DVI 1.0 hosts over a single cable.

The Sil 9011 is capable of receiving and outputting 2 to 8 channels of digital audio of up to 192kHz. An industry-standard I²S port allows direct connection to low-cost audio DACs. An S/PDIF port supports up to 96kHz audio.

Silicon Image's HDMI receivers use the latest generation of PanelLink TMDS core technology. These PanelLink cores pass all HDMI compliance tests.

10.5.1 Features

- HDMI 1.1, HDCP 1.1 and DVI 1.0 compliant receiver
- Integrated PanelLink core supports:
 - DTV resolutions (480i/576i/480p/576p/720p/1080i)
 - PC resolutions (VGA, SVGA, XGA, SXGA, UXGA) up to 165MHz.
- Digital video interface supports video processors:
 - 24-bit and 48-bit RGB/ YCbCr 4:4:4
 - 16/20/24-bit YCbCr 4:2:2
 - 8/10/12-bit YCbCr 4:2:2 (ITU BT.656)
- S/PDIF output supports both IEC 60958 and IEC 67937 for PCM, Dolby Digital, DTS digital or any S/PDIF type audio transmission (32-96kHz Fs)
- Four Programmable I²S outputs for connection to low-cost audio DACs.
- Sample rates up to 192kHz
- Auto audio error detection with programmable soft mute.
- Integrated HDCP decryption engine for receiving protected audio and video content
- Pre-programmed HDCP keys provide highest level of key security, simplifies manufacturing

10.6. 24LC02

10.6.1. General Description

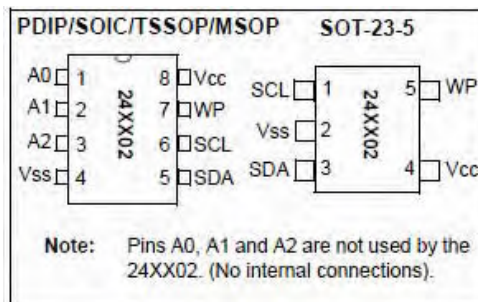
24AA02/24LC02B (24XX02*) is a 2 Kbit Electrically Erasable PROM. The device is organized as one block of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V, with standby and active currents of only 1µA and 1mA, respectively. The 24XX02 also has a page write capability for up to 8 bytes of data.

10.6.2 Features

- Single supply with operation down to 1.8V
- Low-power CMOS technology
 - 1mA active current typical
 - 1µA standby current typical (I-temp)

- Organized as 1 block of 256 bytes (1 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (24AA02) and 400 kHz (24LC02B) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 8 bytes
- 2ms typical write cycle time for page write
- Hardware write-protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP packages
- 5-lead SOT-23 package
- Pb-free finish available
- Available for extended temperature ranges:
 - Industrial (I): -40°C to +85°C
 - Automotive (E): -40°C to +125°C

10.6.3 Pinning



Name	PDIP	SOIC	TSSOP	MSOP	SOT23	Description
A0	1	1	1	1	—	Not Connected
A1	2	2	2	2	—	Not Connected
A2	3	3	3	3	—	Not Connected
Vss	4	4	4	4	2	Ground
SDA	5	5	5	5	3	Serial Address/Data I/O
SCL	6	6	6	6	1	Serial Clock
WP	7	7	7	7	5	Write-Protect Input
Vcc	8	8	8	8	4	+1.8V to 5.5V Power Supply

10.7. μ PA672T

10.7.1. General Description

N-channel Mos-Fet array for switching. The μ PA672T is a super-mini-mold device provided with two MOS FET elements. It achieves high-density mounting and saves mounting costs.

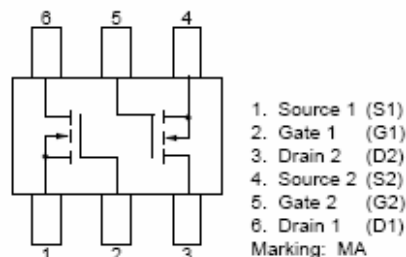
10.7.2. Features

- Two MOS FET circuits in package the same size as SC-70
- Automatic mounting supported

10.7.3 Absolute Maximum Ratings

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	V_{DS}		50	V
Gate to Source Voltage	V_{GS}		± 7.0	V
Drain Current (DC)	$I_{D(C)}$		100	mA
Drain Current (pulse)	$I_{D(pulse)}$	$PW \leq 10 \text{ ms}$, Duty Cycle $\leq 50 \%$	200	mA
Total Power Dissipation	P_T		200 (Total)	mW
Channel Temperature	T_{ch}		150	$^{\circ}\text{C}$
Storage Temperature	T_{stg}		-55 to +150	$^{\circ}\text{C}$

10.7.4 Pinning



10.8. M74HC4052

10.8.1. General Description

The M74HC4052 is a dual four-channel analog MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C2MOS technology and it is pin to pin compatible with the equivalent metal gate CMOS4000B series. It contains 8 bidirectional and digitally controlled analog switches.

10.8.2. Features

- LOW POWER DISSIPATION: $I_{CC} = 4\text{mA}(\text{MAX.})$ at $T_A = 25^{\circ}\text{C}$
- LOGIC LEVEL TRANSLATION TO ENABLE 5V LOGIC SIGNAL TO COMMUNICATE
- WITH $\pm 5\text{V}$ ANALOG SIGNAL
- LOW "ON" RESISTANCE:

70W TYP. ($V_{CC} - V_{EE} = 4.5V$)

50W TYP. ($V_{CC} - V_{EE} = 9V$)

- WIDE ANALOG INPUT VOLTAGE RANGE: $\pm 6V$
- FAST SWITCHING:
tpd = 15ns (TYP.) at $T_A = 25^\circ C$
- LOW CROSSTALK BETWEEN SWITCHES
- HIGH ON/OFF OUTPUT VOLTAGE RATIO
- WIDE OPERATING SUPPLY VOLTAGE RANGE ($V_{CC} - V_{EE}$) = 2V TO 12V
- LOW SINE WAVE DISTORTION: 0.02% at $V_{CC} - V_{EE} = 9V$
- HIGH NOISE IMMUNITY: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 4052

10.8.3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
$V_{CC} - V_{EE}$	Supply Voltage	-0.5 to +13	V
V_I	Control Input Voltage	-0.5 to $V_{CC} + 0.5$	V
$V_{I/O}$	Switch I/O Voltage	$V_{EE} - 0.5$ to $V_{CC} + 0.5$	V
I_{CK}	Control Input Diode Current	± 20	mA
$I_{I/OK}$	I/O Diode Current	± 20	mA
I_T	Switch Through Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	$^\circ C$
T_L	Lead Temperature (10 sec)	300	$^\circ C$

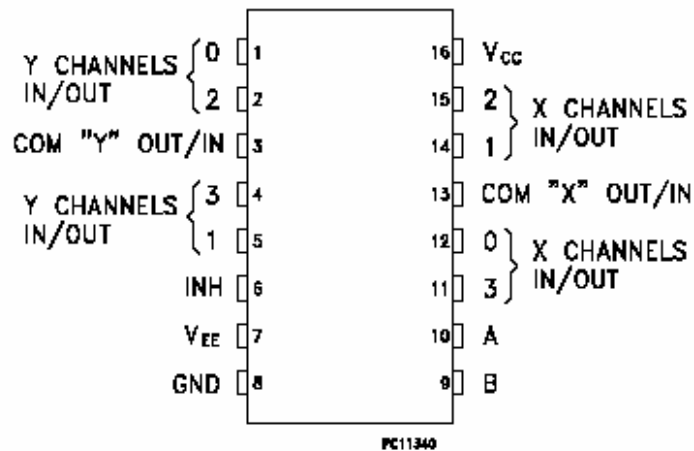
Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

(*) 500mW at $65^\circ C$; derate to 300mW by 10mW/ $^\circ C$ from $65^\circ C$ to $85^\circ C$

10.8.4 Pinning

V_{EE} supply pin is provided for analog input signals. It has an inhibit (INH) input terminal to disable all the switches when high. For operation as a digital multiplexer/demultiplexer, V_{EE} is connected to GND.

A and B control inputs select one channel out of four in each section. All inputs are equipped with protection circuits against static discharge and transient excess voltage.



10.9. Max809

10.9.1. General Description

The MAX809 and MAX810 are cost-effective system supervisor circuits designed to monitor VCC in digital systems and provide a reset signal to the host processor when necessary. No external components are required.

The reset output is driven active within 10 μ sec of VCC falling through the reset voltage threshold. Reset is maintained active for a timeout period which is trimmed by the factory after VCC rises above the reset threshold. The MAX810 has an active-high RESET output while the MAX809 has an active-low RESET output. Both devices are available in SOT-23 and SC-70 packages.

10.9.2. Features

- Precision VCC Monitor for 1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V Supplies
- Precision Monitoring Voltages from 1.2 V to 4.9 V Available in 100 mV Steps
- Four Guaranteed Minimum Power-On Reset Pulse Width Available (1 ms, 20 ms, 100 ms, and 140 ms)
- RESET Output Guaranteed to VCC = 1.0 V.
- Low Supply Current
- Compatible with Hot Plug Applications
- VCC Transient Immunity
- No External Components
- Wide Operating Temperature: -40°C to 105°C
- Pb-Free Packages are Available

10.9.3 Absolute Maximum Ratings

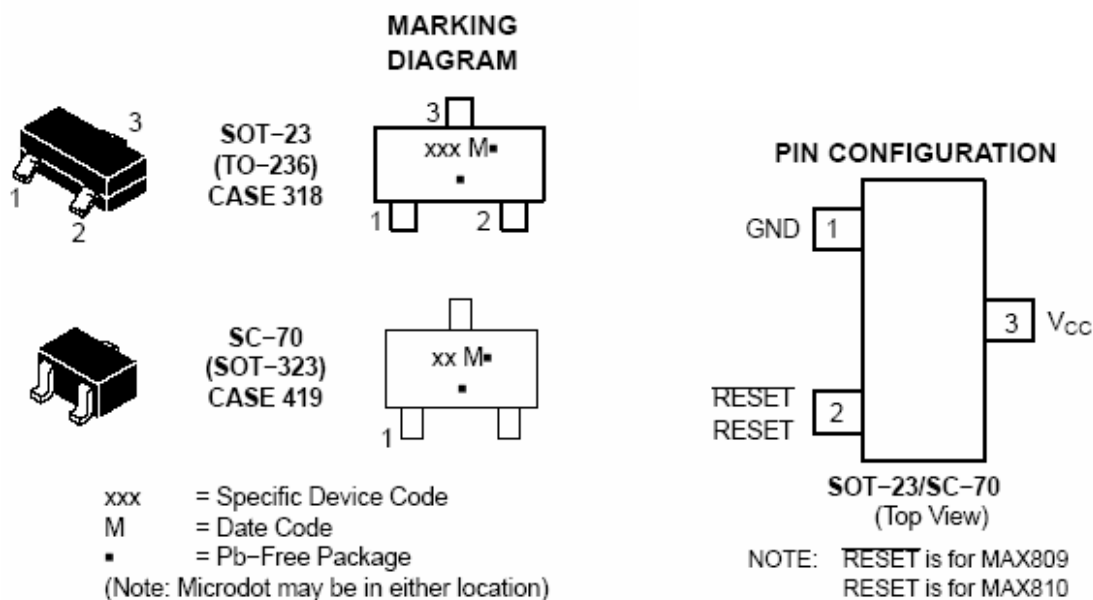
Rating	Symbol	Value	Unit
Power Supply Voltage (V_{CC} to GND)	V_{CC}	-0.3 to 6.0	V
RESET Output Voltage (CMOS)		-0.3 to ($V_{CC} + 0.3$)	V
Input Current, V_{CC}		20	mA
Output Current, RESET		20	mA
dV/dt (V_{CC})		100	V/ μ sec
Thermal Resistance, Junction-to-Air (Note 1)	SOT-23 SC-70 $R_{\theta JA}$	301 314	$^{\circ}\text{C/W}$
Operating Junction Temperature Range	T_J	-40 to +105	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^{\circ}\text{C}$
Lead Temperature (Soldering, 10 Seconds)	T_{sol}	+260	$^{\circ}\text{C}$
ESD Protection Human Body Model (HBM): Following Specification JESD22-A114 Machine Model (MM): Following Specification JESD22-A115		2000 200	V
Latchup Current Maximum Rating: Following Specification JESD78 Class II Positive Negative	$I_{Latchup}$	200 200	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. This based on a 35x35x1.6mm FR4 PCB with 10mm² of 1 oz copper traces under natural convection conditions and a single component characterization.
2. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad \text{with } T_{J(max)} = 150^{\circ}\text{C}$$

10.9.4 Pinning



10.10. 24LC21

10.10.1. General Description

The 24LC21 is a 1K bit electrically erasable programmable memory (EEPROM), organized by 8 bits. This device can operate in two modes: Transmit Only mode and I2C bidirectional mode. When powered, the device is in Transmit Only mode with EEPROM data clocked out from the rising edge of the signal applied on VCLK.

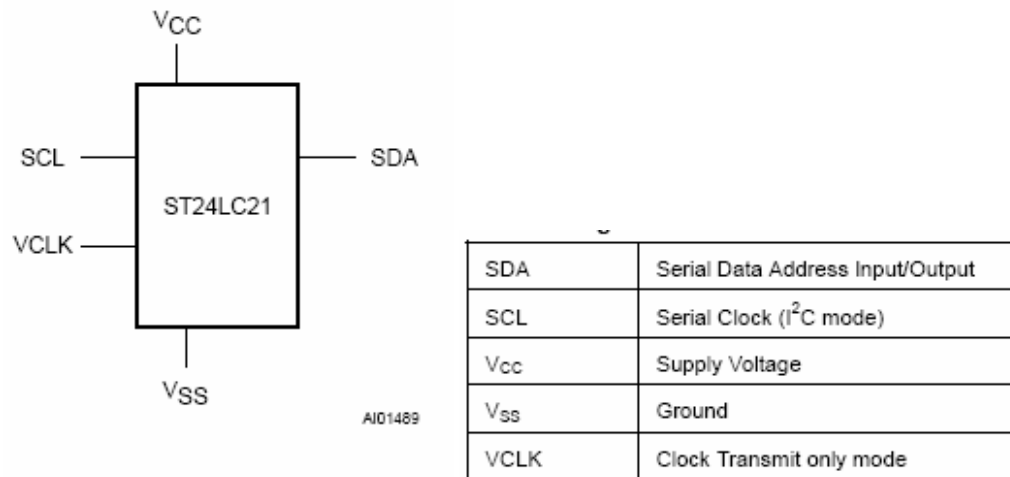
10.10.2. Features

- 1 MILLION ERASE/WRITE CYCLES
- 40 YEARS DATA RETENTION
- 2.5V to 5.5V SINGLE SUPPLY VOLTAGE
- 400k Hz COMPATIBILITY OVER the FULL RANGE of SUPPLY VOLTAGE
- TWO WIRE SERIAL INTERFACE I2C BUS COMPATIBLE
- PAGE WRITE (up to 8 BYTES)
- BYTE, RANDOM and SEQUENTIAL READ MODES
- SELF TIMED PROGRAMMING CYCLE
- AUTOMATIC ADDRESS INCREMENTING
- ENHANCED ESD/LATCH UP PERFORMANCES

10.10.3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T _A	Ambient Operating Temperature grade 1	0 to 70	°C
T _{STG}	Storage Temperature	−65 to 150	°C
T _{LEAD}	Lead Temperature, Soldering (SO8 package) 40 sec (PSDIP8 package) 10 sec	215 260	°C
V _{IO}	Input or Output Voltages	−0.3 to 6.5	V
V _{CC}	Supply Voltage	−0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human Body model) ⁽²⁾	4000	V
	Electrostatic Discharge Voltage (Machine model) ⁽³⁾	500	V

10.10.4 Pinning



11.SERVICE MENU SETTINGS

In order to reach service menu,

- First Press “**MENU**”
- Then press the remote control code, which is “**4725**”

11.1. Video Setup

- **Picture Mute** <.....>
If “Yes” selected, “Picture mute” feature is active.
- **Blue Screen** <.....>
If “Yes” selected, “Blue Background” item is seen in “Feature” menu.
- **YC Delay** <.....>
 - **Tuner PAL** <.....> Value between -8 to+7
 - **Ext PAL** <.....> Value between -8 to+7
 - **SECAM** <.....> Value between -8 to+7
 - **NTSC** <.....> Value between -8 to+7
- **AGC (dB)** <.....> Value between 0 to+8

11.2. AudioSetup

- **Equaliser** <.....>
If “Yes” selected, “Equaliser” item is seen in “Sound” menu.

- **BBE**
- **SRS WOW**
- **Virtual Dolby Surround <.....>**
 If “Yes” selected, Virtual Dolby Surround feature is seen in “**Sound**” menu with selected Virtual Dolby Text.
- **Virtual Dolby Text** The selected item is seen as Virtual Dolby Surround Text.
 - **3DS**
 - **Virtual Dolby**
 - **3D Panorama**
- **AVL <.....>**
 If “Yes” selected, “**AVL**” item is seen in “**Sound**” menu.
- **Carrier Mute <.....>**
 If “Yes” selected, “**Carrier mute**” feature is active.
- **Audio Delay Offset**
- **Prescale**
 - **FM Presc. AVL On <.....>** Value between 0 to +127
 - **AM Presc. AVL On <.....>** Value between 0 to +127
 - **NICAM Presc. AVL On <.....>** Value between 0 to +127
 - **I2S Presc. AVL On <.....>** Value between 0 to +127
 - **SCART Presc. AVL On <.....>** Value between 0 to +127
 - **FM Presc. AVL Off <.....>** Value between 0 to +127
 - **AM Presc. AVL Off <.....>** Value between 0 to +127
 - **NICAM Presc. AVL Off <.....>** Value between 0 to +127
 - **I2S Presc. AVL Off <.....>** Value between 0 to +127
 - **SCART Presc. AVL Off <.....>** Value between 0 to +127
- **Dynamic Bass <.....>**
 If “Yes” selected, “**Dynamic Bass**” item is seen in “**Sound**” menu.
- **Subwoofer <.....>**
 If “Yes” selected, “**Subwoofer**” item is seen in “**Sound**” menu.

11.3. Options 1

- **VCTP Version <.....>**
 - **Basic+**
 - **Basic**
- **Double Digit <.....>**
 If “Yes” selected, “**Double Digit**” button is active for channel selection.
- **TEA6415C Available <.....>**
 If “Yes” selected, video switch IC is active on hardware.
- **TEA642X Available<.....>**
 If “Yes” selected, audio switch IC is active on hardware.
- **Power-Up Mode <.....>**
 - **StandBy** If selected, TV opens in stand by mode.
 - **L.State** If selected, TV opens in Last State mode.
- **TV Open Mode <.....>**
 - **Source**
 - **1st TV**
 - **Last TV**

- **Select Languages <.....>** “Yes” selected languages are seen as option under the “Language” item in “Feature” menu
 - **Language Set 1**
 - **German <.....>**
 - **French <.....>**
 - **Spanish <.....>**
 - **Italian <.....>**
 - **Danish <.....>**
 - **Finnish <.....>**
 - **Swedish <.....>**
 - **Language Set 2**
 - **Greek <.....>**
 - **Norwegian <.....>**
 - **Dutch <.....>**
 - **Portuguese <.....>**
 - **Polish <.....>**
 - **Turkish <.....>**
 - **Russian <.....>**
 - **Czech <.....>**
 - **Language Set 3**
 - **Hungarian <.....>**
 - **Slovak <.....>**
 - **Slovenian <.....>**
 - **Romanian <.....>**
 - **Bulgarian <.....>**
 - **Croatian <.....>**
 - **Serbian <.....>**
 - **Hebrew <.....>**
- **First APS <.....>**

If “Yes” selected, first time TV opens by asking APS.
- **APS Volume <.....>** value between 0 to +63
- **Burn In Mode <.....>**

If “Yes” selected, TV opens with Burn-In mode. This mode is used in manufacturing.
- **APS Test**
- **HDMI WP <.....>**

If “Yes” selected, HDMI EDID ROM is write protected.

11.4. Options 2

- **Autostore <.....>**

If “Yes” selected, Channel is automatically stored.
- **Led Type <.....>**
 - **1 Led 1 Colour**
 - **1 Led 2 Colours**
 - **2 Led 2 Colours**
- **PC PIP <.....>**
- **PC Stand By <.....>**

11.5. Service Scan/Tuning Setup

- **Search for L/L' <.....>**
- **Pref. Search Standard <.....>**
 - **BG, DK, I**
 - **L/L'**
 - **M**
- **Station Ident <.....>**
- **ATS Delay Time (ms) <.....>** Value between 20 to 250
- **Color Killer Threshold <.....>** Value between 0 to +255
- **Tuner Options <.....>**
 - **Control Byte <.....>** Value between 0 to +255
 - **Low-Mid – Low Byte <.....>** Value between 0 to +255
 - **Low-Mid – High Byte <.....>** Value between 0 to +255
 - **Mid-High – Low Byte <.....>** Value between 0 to +255
 - **Mid-High – High Byte <.....>** Value between 0 to +255
 - **BSW1 <.....>** Value between 0 to +255
 - **BSW2 <.....>** Value between 0 to +255
 - **BSW3 <.....>** Value between 0 to +255

11.6. External Source Settings

- **DTV <.....>**
- **DVD <.....>**
- **Ext 2 S-Video <.....>**
- **Ext 3 <.....>**
- **Ext 3 S-Video <.....>**
- **FAV <.....>**
- **BAV <.....>**
- **S-Video <.....>**
- **HDMI 1 <.....>**
- **HDMI 2 <.....>**
- **YPbPr <.....>**
- **PC <.....>**

11.7. Picture Mode

- **Sources <.....>**
 - **Tuner**
 - **CVBS**
 - **RGB**
 - **SVHS**
 - **HDMI**
 - **YPbPr**
 - **PC**
 - **PIP**
- **Picture Mode <.....>**
 - **Dynamic**
 - **Natural**
 - **Cinema**

- x **Colour Temp** <.....>
 - ③ **Cool**
 - ③ **Normal**
 - ③ **Warm**
- x **Contrast** <.....> *Value between 0 to +63*
- x **Brightness** <.....> *Value between 0 to +63*
- x **Sharpness** <.....> *Value between 0 to +15*
- x **Colour** <.....> *Value between 0 to +63*
- x **Backlight** <.....> *Value between 0 to +255*
- x **R** <.....> *Value between -63 to +63*
- x **G** <.....> *Value between -63 to +63*
- x **B** <.....> *Value between -63 to +63*

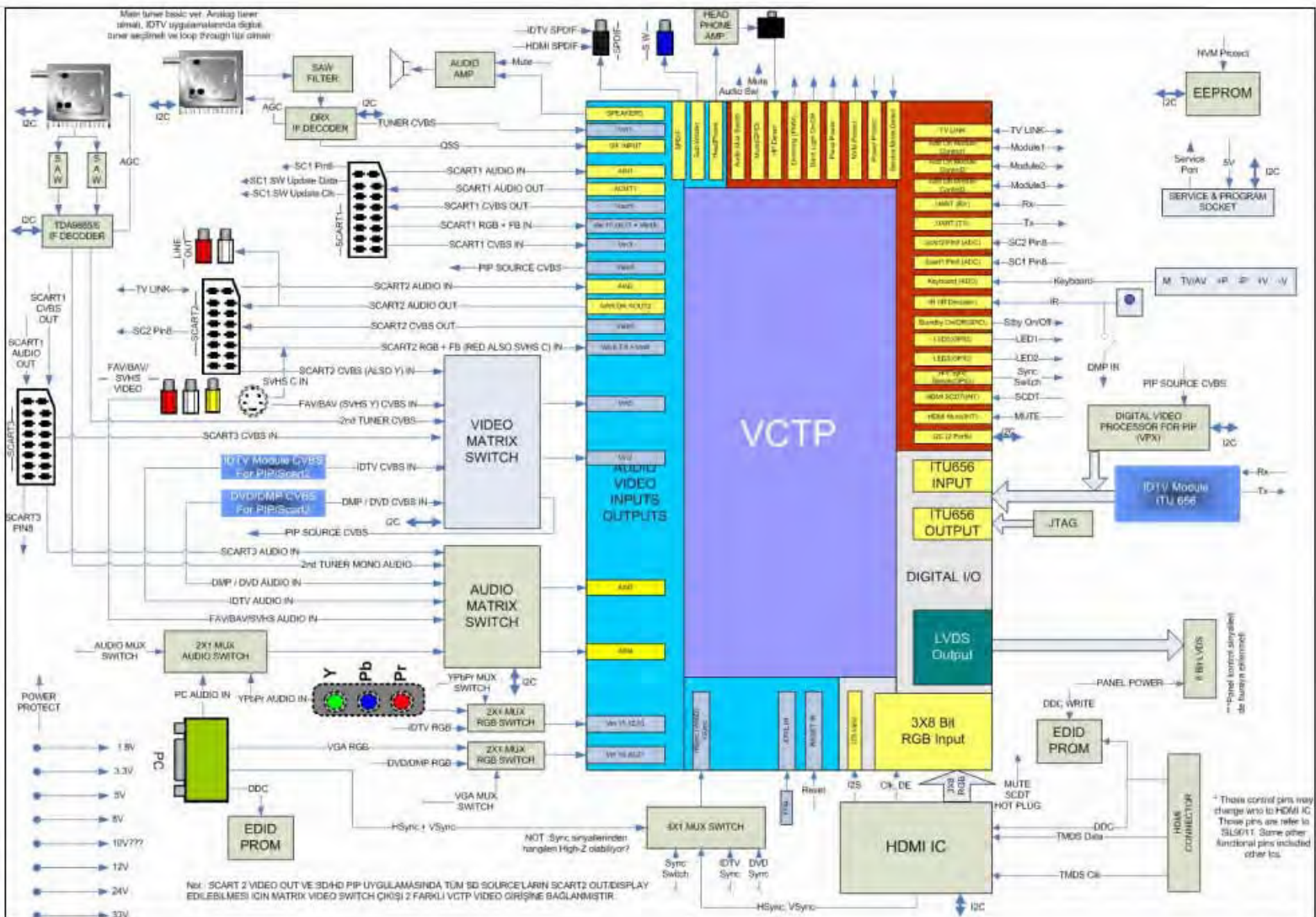
11.8. Reset TV-Set

- x **Initialise NVM from ROM**
Press green button to reset the NVM from ROM

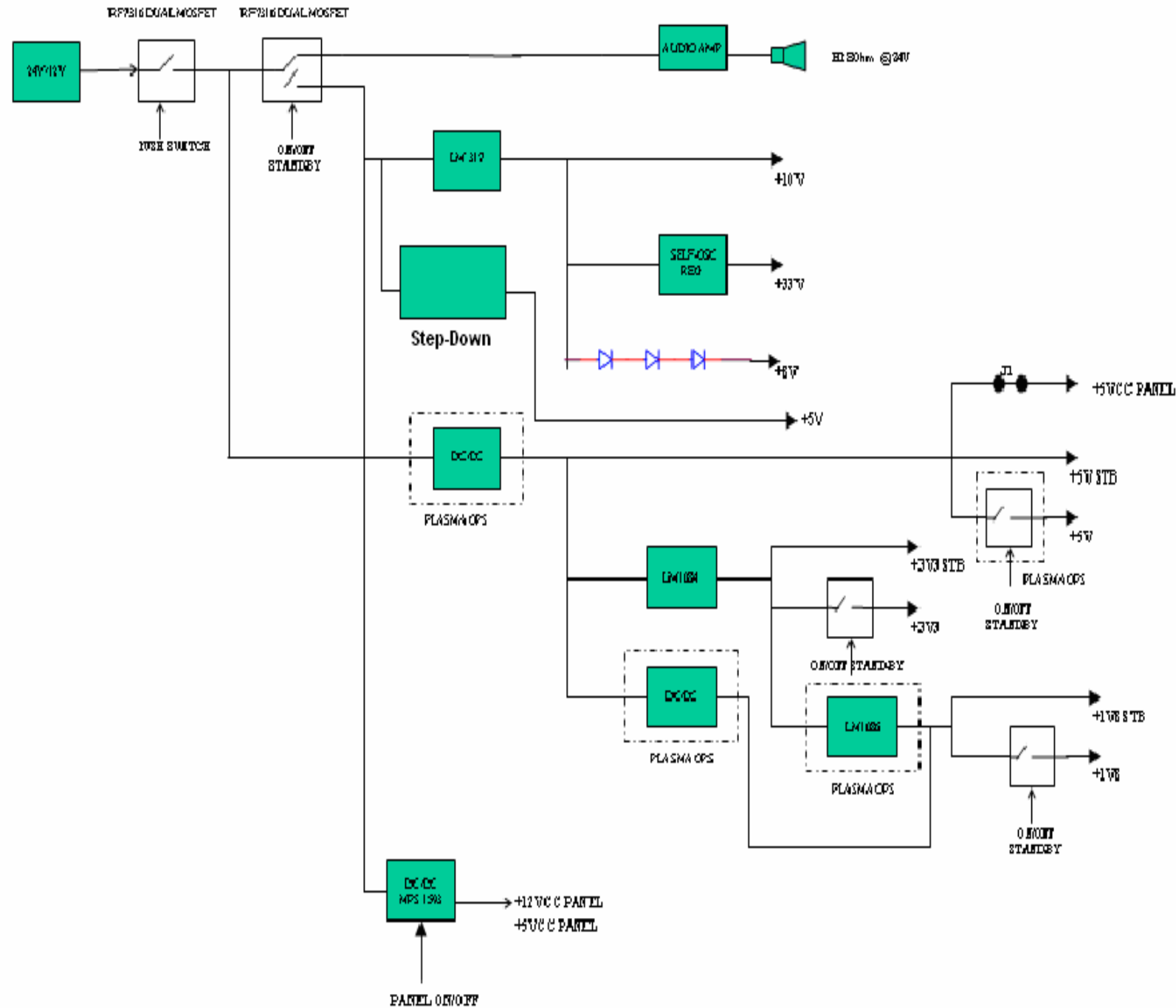
12. TROUBLESHOOTING GUIDE

NO	DEFECT APPEARANCE	DEFECT IDENTIFICATION AND SOLUTIONS
1	When the TV is operated for the first time, STANDBY LED lights but the TV switches on	IC403 E2Epron is plugged empty, after the programming process of the first values has finished, TV will switch on by itself.
2	Standby LED does not ligh ever.	Are there 3.3V on IC001's bottomright pin? If no, 3.3V are not drawing in, there can be an error in PW board; underneath VCTP, SMD material can be disintegrated. Are there 1.8V in IC001 solder area? If no, 1.8V are not drawing in; IC001 can be defective or underneath VCTP, SMD material can be disintegrated. Are there 3.3V on IC406's top left pin? If no, IC406 can be defective. Are there 1.8V on S719? If no, IC001 can be defective. Are there 3.3V on S700? If no, there can be an error in PW board.
3	Standby LED does not light and/or IR receiver does not work.	Are there 5V on pin PL409 5? If no, there can be a problem in PW board or SMD material can be disintegrated.
4	Picture is available but there is no sound.	Are there 24V on the pin, which is indicated as number 1, of PL001 socket. If no, there can be a problem in PW board. L603 can be cold soldering.
5	Sound is available but there is no picture.	PL406 can be cold soldering. Is there display voltage in Q005's top points? (for LG 12V, for other displays 5V). If no; L007 for LG, L006 for other displays can be unplugged. Q005 can be defective.
6	Neither picture nor sound is available.	Are there 5V in 7th pin of tuner? If no, IC007 and surrounding equipment can be defective, L101 can be defective. Are there 33V in 9th pin of tuner? If no, there can be a problem in PW board. Are there 3.3V in L104 inductor? If no, there can be a problem in PW board. Are there 12V in pin 8 of the PL003 socket? If no, there can be a problem in PW board. Q410 and Q411 can be defective. Are there 10V in the mid pin of IC004? If no, IC004 can be defective. Are there 8V on L200? If no, there can be a problem in D004, D005, D006 or there could be cold soldering.
7	TV switches on but constantly switches to HDMI input. While trying to tune a channel, always switches to C05.	Are there 1.8V on S719? If no, IC001 can be defective. Are there 3.3V on S700? If no, PW board can be defective. IC702 can be defective. S705 and S706 can be cold soldering.
8	No sound from PC or YPbPr.	IC905 or surrounding equipment can be defective. IC 905 supply voltage may not be drawing in 10V.
9	TFT backlight level cannot be controlled, it's level is fixed.	Q002, Q003, 1006 or surrounding eqipment can be defective or SMD material can be disintegrated.
10	TV switches on; however, after a short break, it switches off again by itself.	When the TV is switched on; there should be displayed voltages as following: 5V on C074, 3.3V on PL004 pin 4, 8V on IC004 mid pin and Q005 top points. If one is missing, TV may shut down after a short while after it is switched on.

13.1. General Block Diagram

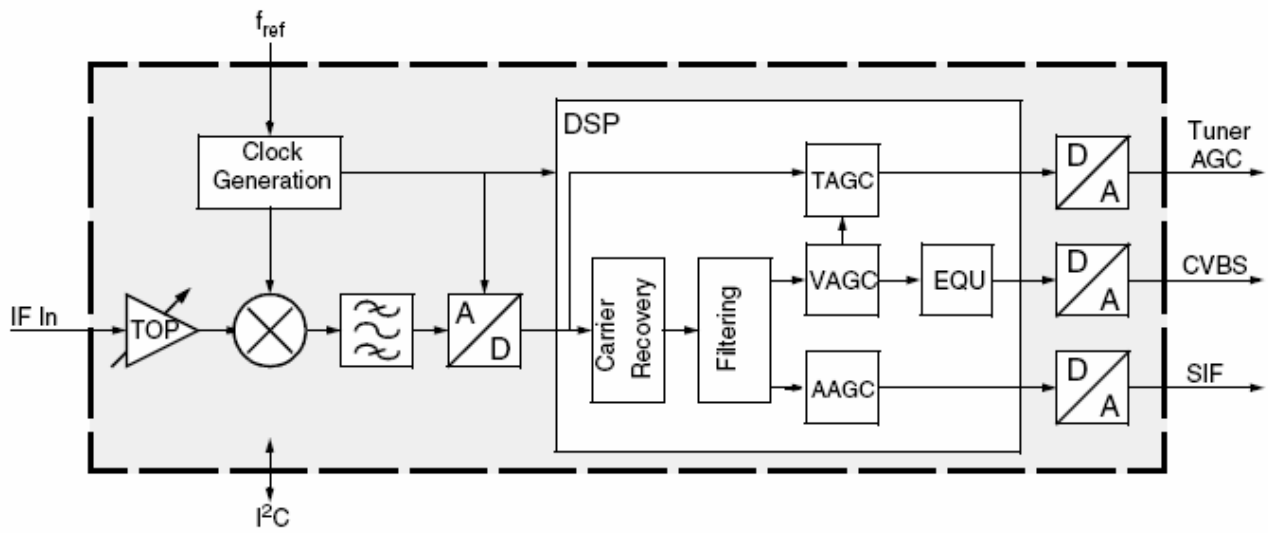


17MB22 POWER MANAGEMENT DIAGRAM



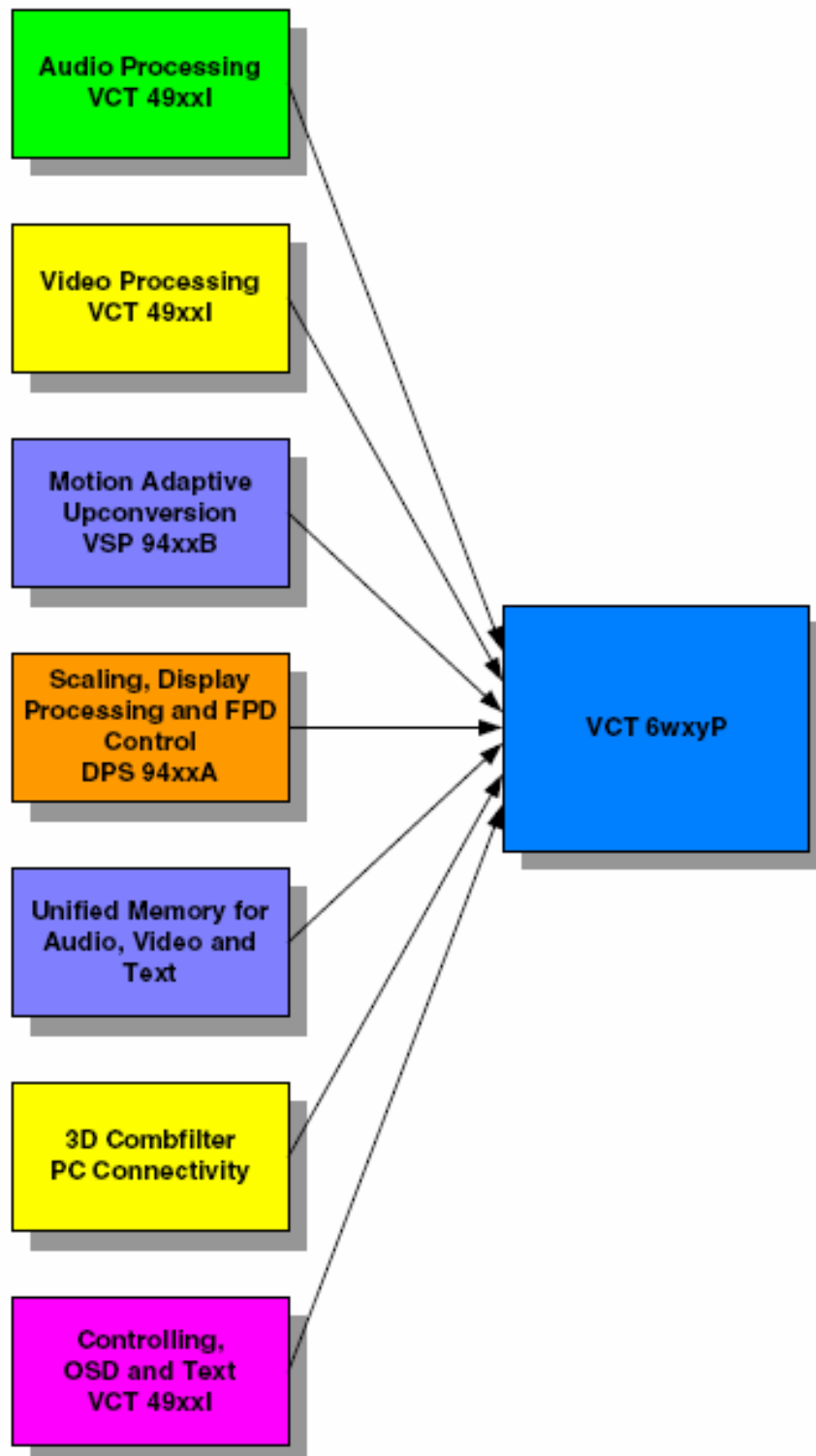
13.2. Power Management

13.3. DRX (IF Demodulator) Block Diagram

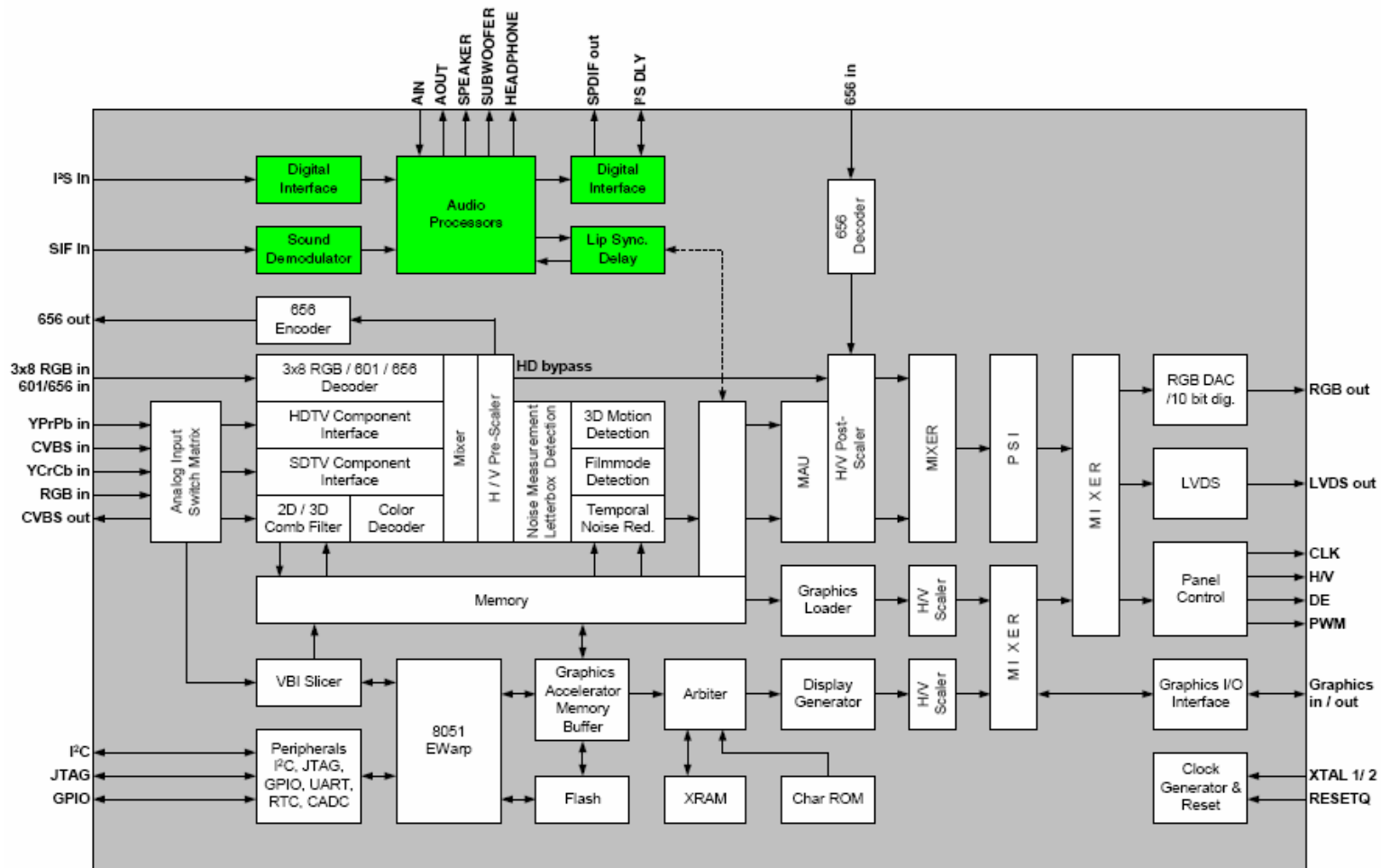


13.4. VCTP

14.4.1. General Block Diagram

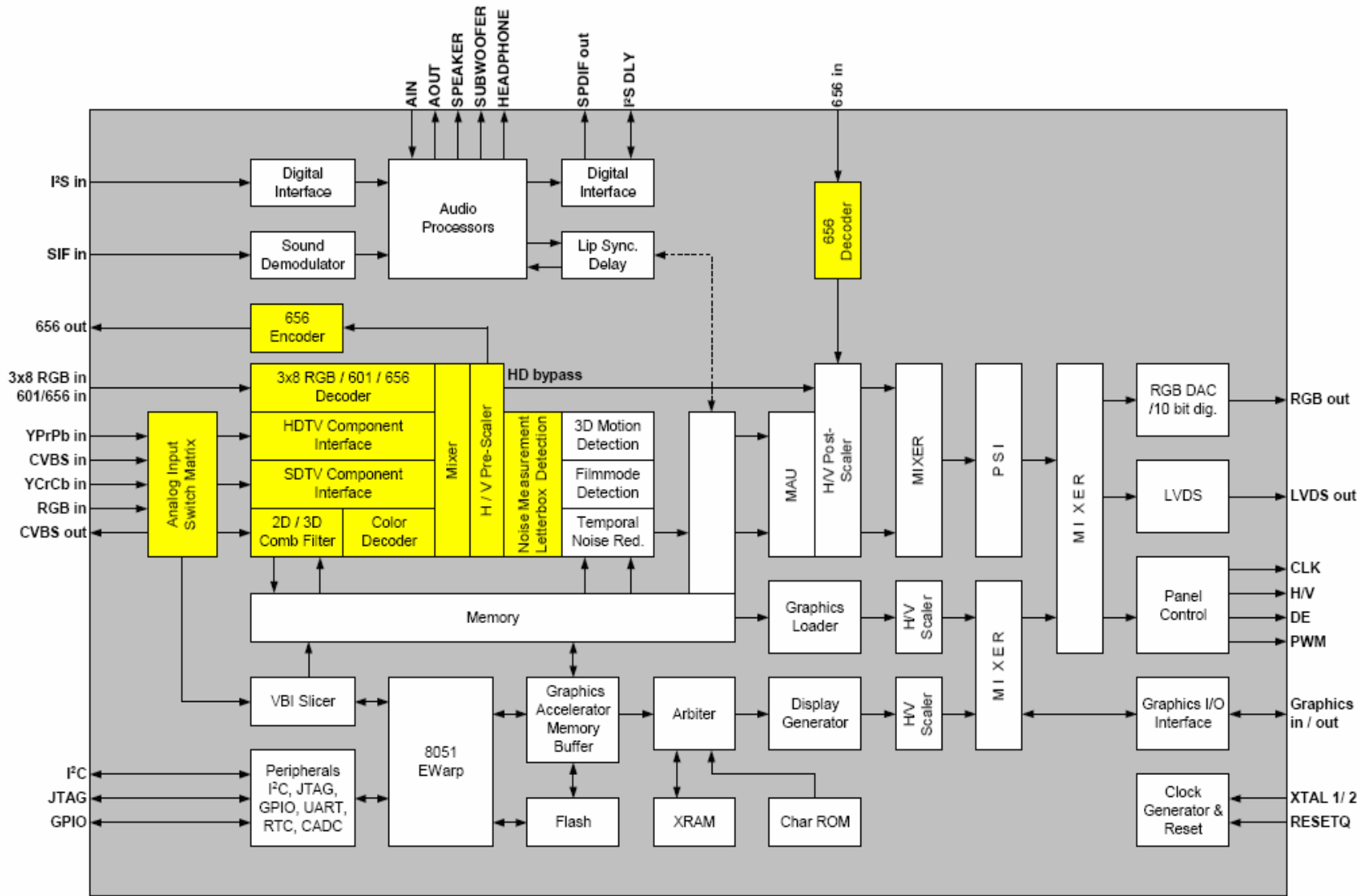


13.4.2. MSP Block Diagram



13.4.3

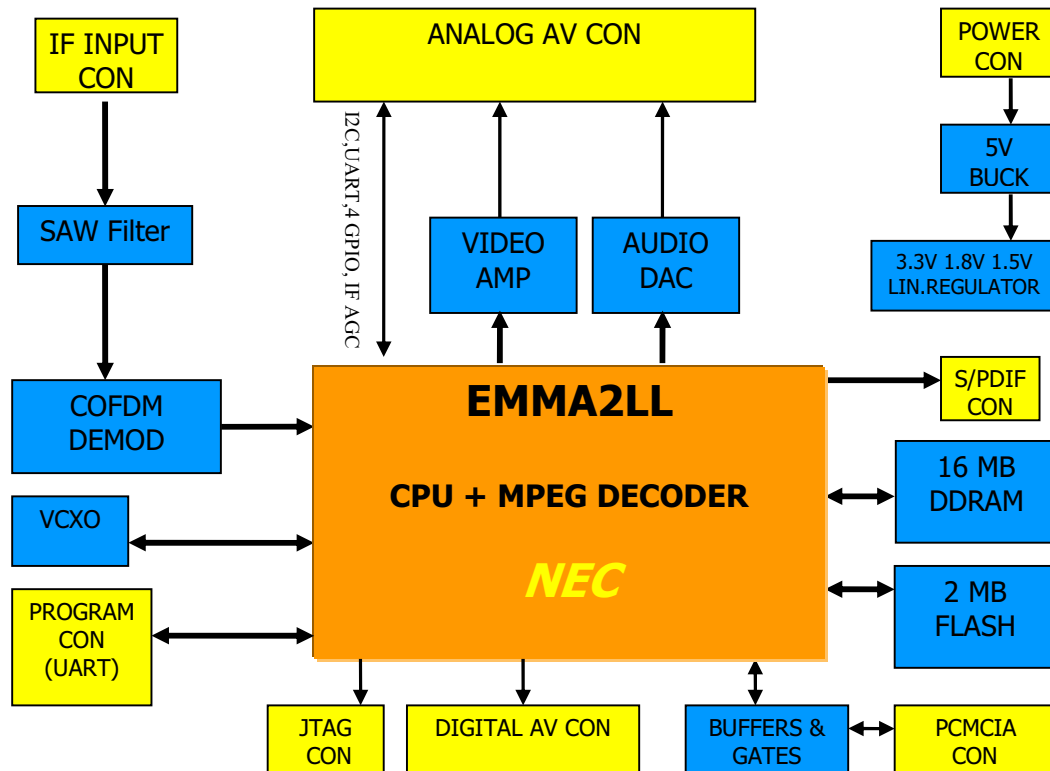
Video Processor of VCT 6wxyp Block Diagram



13.5. TDM1300 HARDWARE DESCRIPTION (IDTV)

Item	Description
PCB	4-layer
MPEG decoder	EMMA2LL (NEC)
FLASH	29LV160TE (Spansion, Eon) 2MB
DDRAM	EDD1216AATA (Elpida, Nanya) 16MB
Audio DAC	CS4335 (Crystal)
Video AMP	FMS6145 (Fairchild)
COFDM Demodulator	DRX3973D (Micronas)
Tuner	DTT7103 (Thomson) DTOS401TH17XA (Samsung)
VCXO	PI6CX100-27 (Pericom)
Buck Regulator	MP1593 (MPS)
3.3V Regulator	NCP1117-3.3V (Onsemi)
1.8V Regulator	NCP1117-1.8V (Onsemi)
1.5V Regulator	NCP1117-1.5V (Onsemi)
74LVC16244 (x4)	16-bit buffer with OE (Various)
74LVC245	Octal Bus Transceiver (Various)
74LVC00	NAND Gate (Various)

13.5.1 IDTV Module Block Diagram



14. CONNECTORS

14.1. *POWER Connector*

Pin	Description
1	+12/24V
2	+12/24V
3	GND
4	GND

14.2. *EMMA2LL JTAG Connector*

Pin	Description
1	GND
2	JTCLK
3	3.3V
4	JTDO
5	NC
6	JTMS
7	NC
8	JTRST
9	GND
10	JTDI

14.3. *ANALOG AV Connector*

Pin	Description	Pin	Description
1	DVB_SCL	13	GND
2	DVB_SDA	14	GND
3	GND	15	DVB_R_AUDIO
4	GND	16	DVB_L_AUDIO
5	IRQ	17	GND
6	DVB_RX	18	DVB_IN_CVBS
7	DVB_TX	19	GND
8	GPIO4	20	DVB_IN_B / DVB_IN_C
9	GPIO3	21	GND
10	GPIO2	22	DVB_IN_G / DVB_IN_Y
11	GPIO1	23	GND
12	IF_AGC_DVB	24	DVB_IN_R

14.4. IF Connector

Pin	Description
1	IF +
2	IF -
3	GND

14.5. PROGRAMMING Connector

Pin	Description
1	TXD
2	GND
3	RXD

14.6. S/PDIF Connector

Pin	Description
1	S/PDIF
2	GND

14.7. DIGITAL AV Connector

Pin	Description	Pin	Description
1	I2S Word Select	11	GND
2	I2S Serial Clock	12	Digital Video Pixel Clock
3	I2S Serial Data	13	Digital Video Y/Cb/Cr DATA7
4	GND	14	Digital Video Y/Cb/Cr DATA6
5	GND	15	Digital Video Y/Cb/Cr DATA5
6	GND	16	Digital Video Y/Cb/Cr DATA4
7	Internal Vertical SYNC	17	Digital Video Y/Cb/Cr DATA3
8	Internal Horizontal SYNC	18	Digital Video Y/Cb/Cr DATA2
9	GND	19	Digital Video Y/Cb/Cr DATA1
10	GND	20	Digital Video Y/Cb/Cr DATA0

14.8. PCMCIA Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	35	GND	Ground
2	D3	Data bit 3	36	CD1#	Card Detect
3	D4	Data bit 4	37	MDO3	MPEG Data Out 3
4	D5	Data bit 5	38	MDO4	MPEG Data Out 4
5	D6	Data bit 6	39	MDO5	MPEG Data Out 5
6	D7	Data bit 7	40	MDO6	MPEG Data Out 6
7	CE1#	Card Enable	41	MDO7	MPEG Data Out 7
8	A10	Address bit 10	42	CE2#	Card Enable
9	OE#	Output Enable	43	VS1#	Voltage Sense 1
10	A11	Address bit 11	44	IORD#	I/O Read
11	A9	Address bit 9	45	IOWR#	I/O Write
12	A8	Address bit 8	46	MISTRT	MPEG Data In Start
13	A13	Address bit 13	47	MDI0	MPEG Data In 0
14	A14	Address bit 14	48	MDI1	MPEG Data In 1
15	WE#	Write Enable	49	MDI2	MPEG Data In 2
16	IREQ#	Interrupt Request	50	MDI3	MPEG Data In 3
17	VCC	Supply Voltage	51	VCC	Supply Voltage
18	VPP	Programming and Peripheral Supply	52	VPP	Programming and Peripheral Supply
19	MIVAL	MPEG Data In Valid	53	MDI4	MPEG Data In 4
20	MCLKI	MPEG Data Clock Input	54	MDI5	MPEG Data In 5
21	A12	Address bit 12	55	MDI6	MPEG Data In 6
22	A7	Address bit 7	56	MDI7	MPEG Data In 7
23	A6	Address bit 6	57	MCLKO	MPEG Data Clock Output
24	A5	Address bit 5	58	RESET	Card Reset
25	A4	Address bit 4	59	WAIT#	Extend bus cycle
26	A3	Address bit 3	60	INPACK#	Input Port Acknowledge
27	A2	Address bit 2	61	REG#	Register select & I/O Enable
28	A1	Address bit 1	62	MOVAL	MPEG Data Out Valid
29	A0	Address bit 0	63	MOSTRT	MPEG Data Out Start
30	D0	Data bit 0	64	MDO0	MPEG Data Out 0
31	D1	Data bit 1	65	MDO1	MPEG Data Out 1
32	D2	Data bit 2	66	MDO2	MPEG Data Out 2
33	IOIS16#	I/O Port Is 16-bit	67	CD2#	Card Detect
34	GND	Ground	68	GND	Ground

15. CONCEPT ICs

15.1. *μPD61115*

15.1.1 Description

The *μPD61115* device is a member of the second generation of multimedia processors based on NEC's Enhanced MultiMedia Architecture (EMMArchitecture). These devices provide nearly all the functionality required to realise a high performance and cost-effective digital set-top box or integrated digital TV.

15.1.2 Features

- MPEG1 and MPEG2-TS/PS compliant
- High performance MIPS32™ 4Kc™ main CPU core
- High performance MIPS32™ 4Km™ sub-CPU core
- Integrated DVB descrambling with family options for Irdeto and Multi2
- 36 PID filters, 32 section filters
- Video Outputs: 4 DACs for RGB, Component video, S-video and composite output with support for PAL, NTSC and SECAM
- 4 graphics planes
- Audio Output: 2-channel PCM and SPDIF
- Peripherals support
 - two fast UARTs with 16byte FIFOs
 - I2C interface
 - infrared receiver
 - three wire clocked serial interface
- System timers, RTC and Watchdog timer
- Motorola/Intel Bus.

15.2. *DRX 3973D*

Fourth-Generation COFDM Demodulators

15.2.1 Introduction

The DRX 3973D and the DRX 3977D are fourth-generation COFDM demodulators that offer today's highest level of front-end integration resulting in ultimate DVB-T digital reception, compliant to ETS 300 744, DTG D-Book, EICTA E-Book, and Nordig Unified v1.0.2 .

The DRX 3973/77D applies cutting-edge digital filtering techniques in combination with a high-performance A/D-converter and PLL configuration, resulting in superior performance figures in the presence of digital and analog adjacent channels.

Progressive channel estimator algorithms provide exceptional performance in multipath- and dynamic echo conditions – an especially important feature for single-frequency networks and indoor reception.

The state-of-the-art impulsive noise cruncher suppresses interferences originating from sources such as cars, electrical motors, and household appliances.

15.2.2 Features

- ❖ Highest level of front-end integration and flexibility:
 - Integrated PGA (programmable gain amplifier) 30 dB
 - Single 8 MHz SAW filter operation
 - 2 AGC control signals available for RF and IF amplifier control
 - Flexible clock reference options
 - Re-use of 4 MHz tuner clock reference
 - Pre-SAW sense input for optimal RF AGC setting and RF-level measurement
- ❖ Excellent digital reception performance:
 - Superior digital and analog adjacent channel performance (> -40 dB for QEF)
 - Impulsive noise cruncher
 - Multipath and dynamic echoes
- ❖ The input IF frequency ranging up to 44 MHz ensures upward compatibility for new tuner topologies
- ❖ Integrated microprocessor to perform autonomous detection and operation of all possible DVB-T modes, without interaction with the host processor
- ❖ Fully automatic and fast signal acquisition: UHF and VHF band-scan in <20 seconds
- ❖ Meets all international DVB-T receiver specifications: NORDIG Unified, DTG, EICTA
- ❖ Comfortable software drivers for integration of tuner and COFDM demodulator
- ❖ Secondary serial interface for tuner control
- ❖ 5 V tolerant AGC and secondary serial protocol outputs
- ❖ 2 general purpose I/O pins (GPIO)
- ❖ Configurable parallel or serial MPEG-TS output
- ❖ PMQFP64-2 package: footprint 10·10 mm (DRX 3973D)
- ❖ PQFN48-1 package: small footprint 7·7 mm (DRX 3977D)
- ❖ IEEE 1149.1 boundary scan

15.2.3 Applications

- ❖ IDTV / hybrid TV
- ❖ Set-top boxes
- ❖ PVR / DVDR
- ❖ Network interface modules (NIM)
- ❖ PC-TV applications

15.3. PI6CX100-27

27 MHz 3.3V VCXO for Set-Top Box Applications

15.3.1 Features

- 3.3V operating voltage
- Uses an inexpensive external crystal
- On-chip VCXO with pull range of 240ppm
- VCXO tuning voltage from 0 to 3.3V
- 10mA output drive at CMOS levels
- Available in SOIC package

15.3.2 Description

The PI6CX100-27 is a low-cost, high-performance 3.3V VCXO, designed to replace expensive VCXO modules. The on-chip Voltage Controlled Crystal Oscillator accepts a 0 to 3.3V input voltage to cause clocks to vary by ± 120 ppm. This device uses an inexpensive external pullable crystal at 27 MHz to produce the same output frequency. The PI6CX100-27 is designed for Set-Top Box applications.

15.4. 74V1G08

SINGLE 2-INPUT AND GATE

- ❖ HIGHSPEED: $t_{PD} = 4.3$ ns (TYP.) at $V_{CC} = 5V$
- ❖ LOWPOWERDISSIPATION:
 - $I_{CC} = 1$ μA (MAX.) at $T_A = 25$ °C
- ❖ HIGHNOISEIMMUNITY:
 - $V_{NIH} = V_{NIL} = 28\%V_{CC}$ (MIN.)
- ❖ POWERDOWN PROTECTIONON INPUTS
- ❖ SYMMETRICAL OUTPUT IMPEDANCE:
 - $|I_{OH}| = I_{OL} = 8$ mA (MIN)
- ❖ BALANCEDPROPAGATIONDELAYS:
 - $t_{PLH} \cong t_{PHL}$
- ❖ OPERATINGVOLTAGERANGE:
 - V_{CC} (OPR) = 2V to 5.5V
- ❖ IMPROVEDLATCH-UP IMMUNITY

16.4.1 Description

The 74V1G08 is an advanced high-speed CMOS SINGLE 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C2MOS technology.

15.5. FMS6145

Low Cost Five Channel 4th Order Standard Definition Video Filter Driver

15.5.1 Features

- Five fourth-order 8MHz (SD) filters
- Transparent input clamping
- Dual video load drive (2Vpp, 75 Ω)
- AC or DC-coupled inputs
- AC or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Lead (Pb) Free TSSOP-14 package

15.5.2 Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- HDTV
- Personal video recorders (PVR)
- Video on demand (VOD)

15.5.3 Description

The FMS6145 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Five 4th order filters provide improved image Quality compared to typical 2nd or 3rd order passive solutions.

The FMS6145 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required.

The outputs can drive AC or DC-coupled single (150Ω) or dual(75Ω) loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels will be offset approximately +280mV at the output.

15.6. *MP1593*

3A, 28V Step-Down Converter

15.6.1 Description

The MP1593 is a step-down regulator with an internal Power MOSFET. It achieves 3A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilisation. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown. Adjustable soft-start reduces the stress on the input source at turn-on. In shutdown mode the regulator draws 20 μ A of supply current.

The MP1593 requires a minimum number of readily available external components to complete a 3A step down DC to DC converter solution.

15.6.2 Features

- 3A Output Current
- Programmable Soft-Start
- 100m Ω Internal Power MOSFET Switch
- Stable with Low ESR Output Ceramic Capacitors
- Up to 95% Efficiency
- 20 μ A Shutdown Mode
- Fixed 385KHz Frequency

- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Wide 4.75 to 28V Operating Input Range
- Output Adjustable from 1.22Vs
- Under Voltage Lockout
- Available in 8-Pin SOIC Package

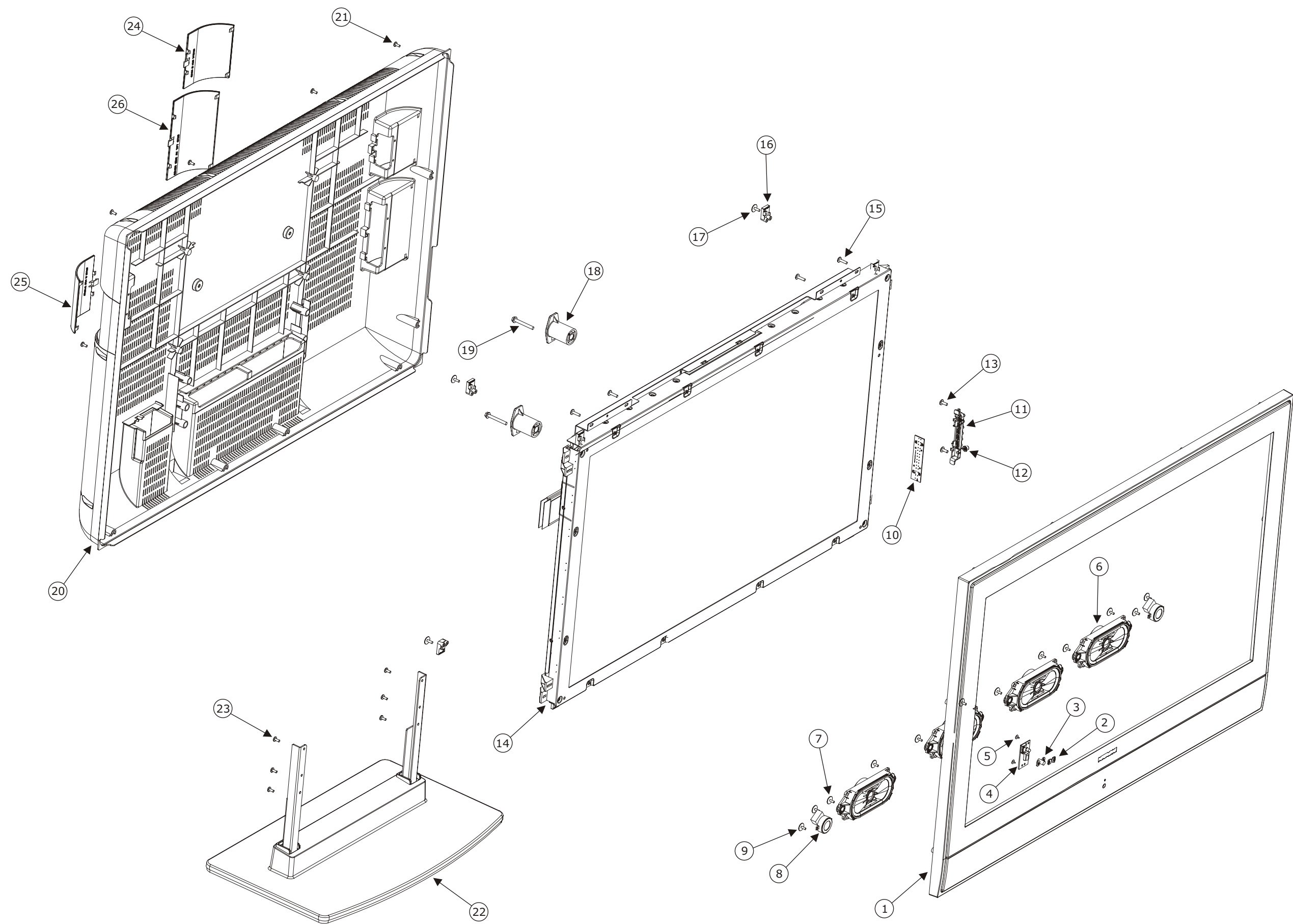
15.6.3 Applications

- Distributed Power Systems
- Battery Chargers
- Pre-Regulator for Linear Regulators
- Flat Panel TVs
- Set-Top Boxes
- Cigarette Lighter Powered Devices
- DVD/PVR Devices

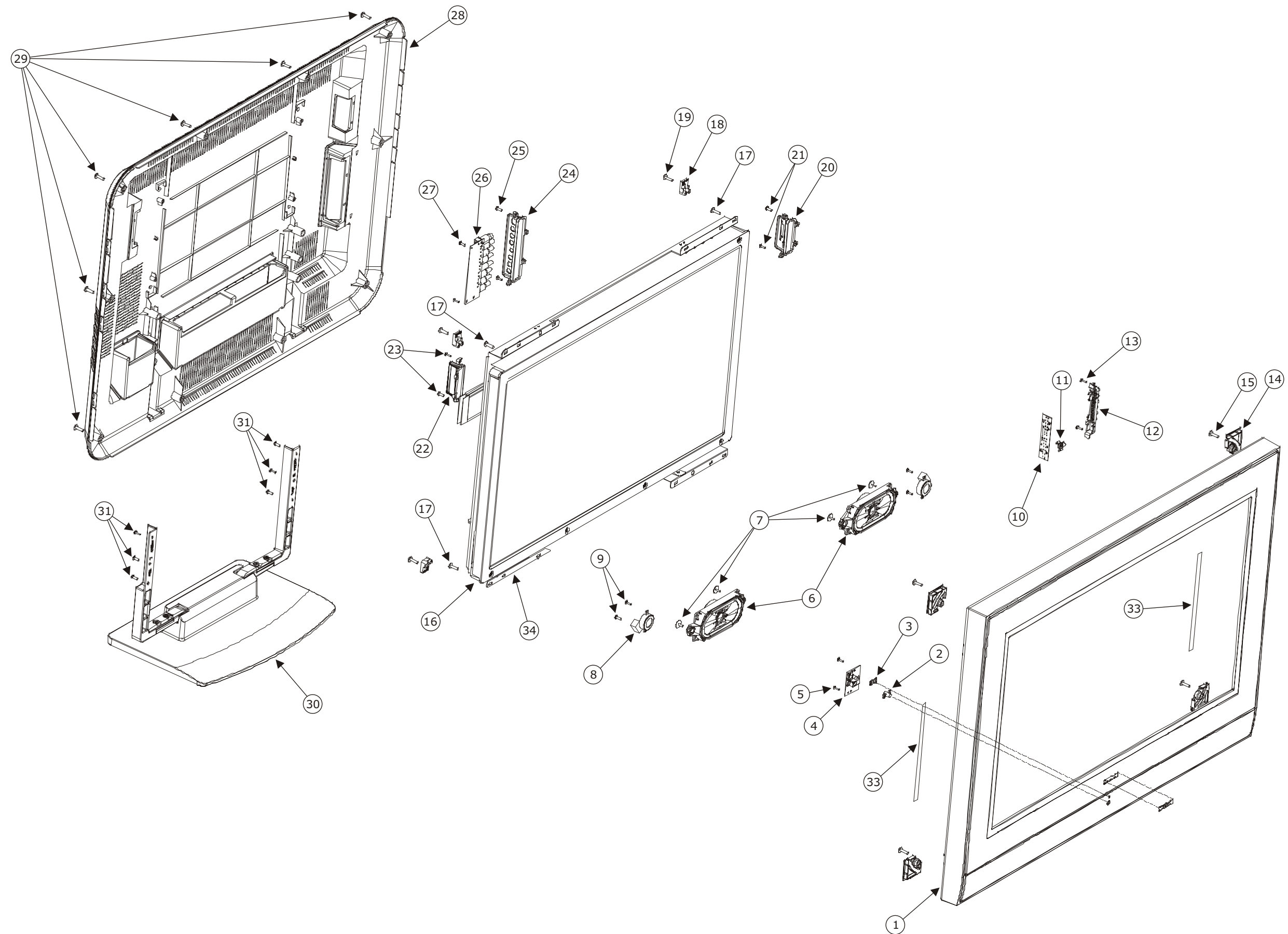
16. REPLACEMENT PARTS

**THE UPDATED PARTS LIST
FOR THIS MODEL IS
AVAILABLE ON ESTA**

17. ASSEMBLY DRAWING [For 37-inch models ONLY]



[For 32-inch models ONLY]

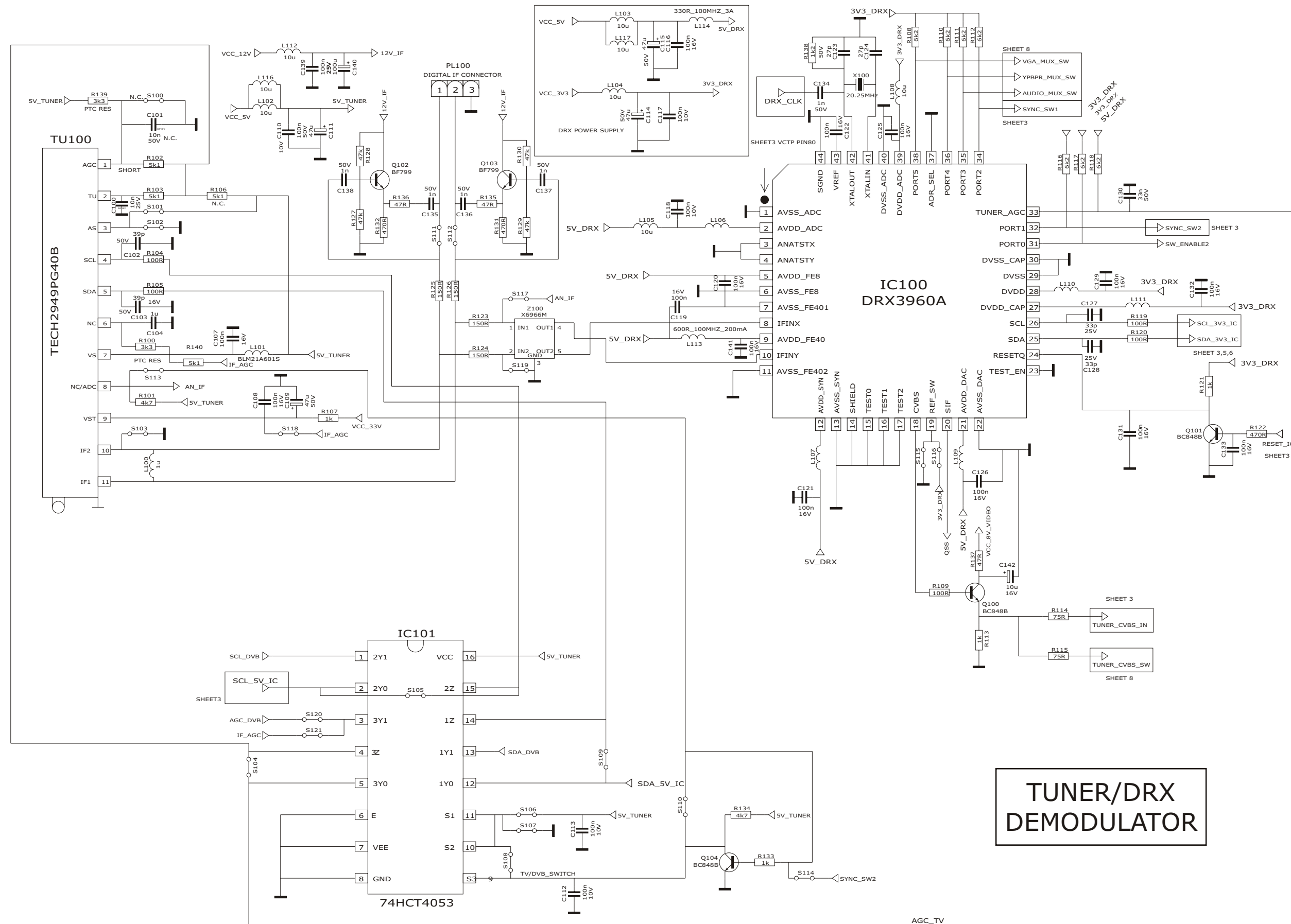


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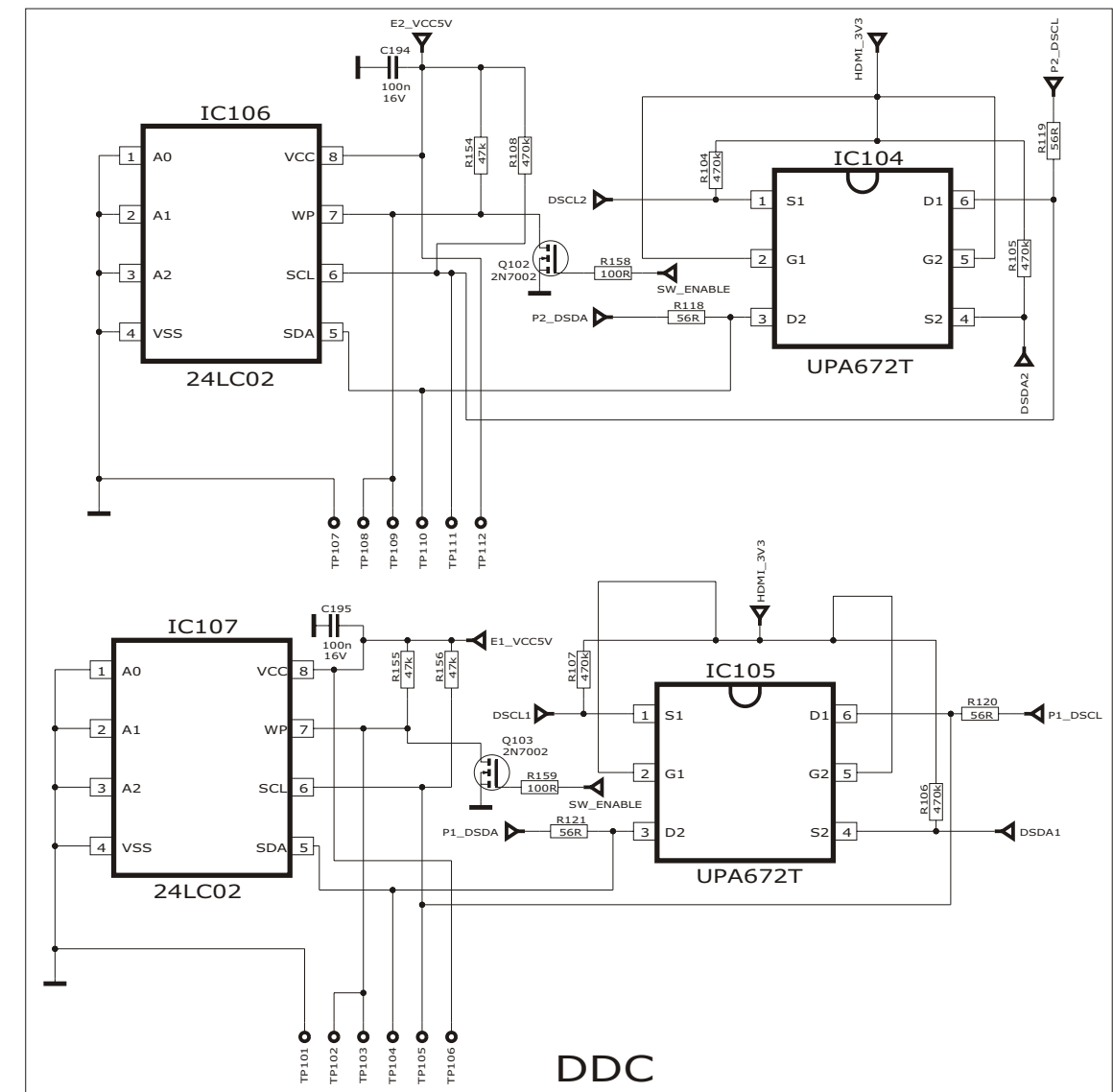
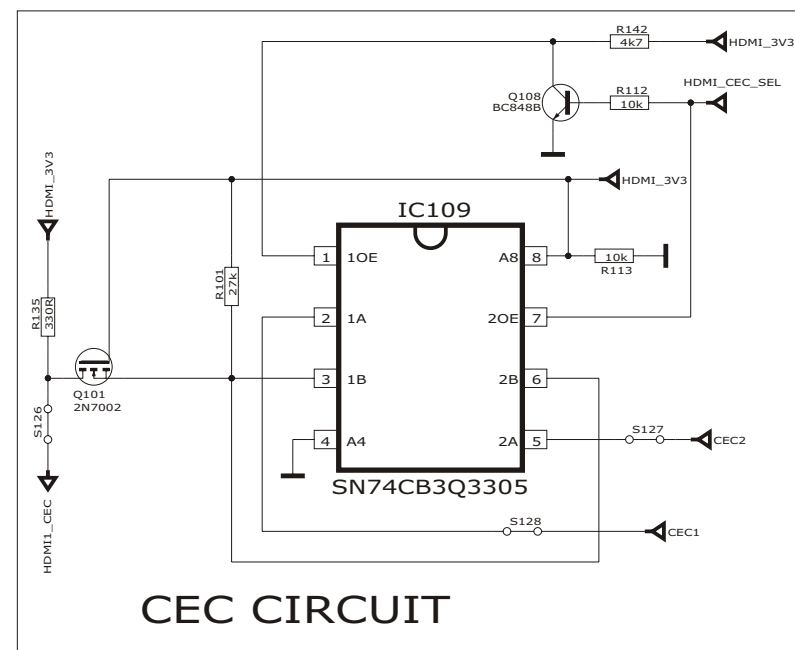
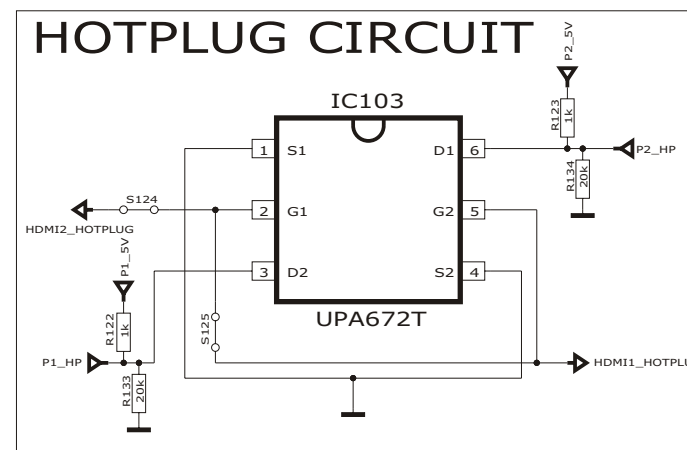
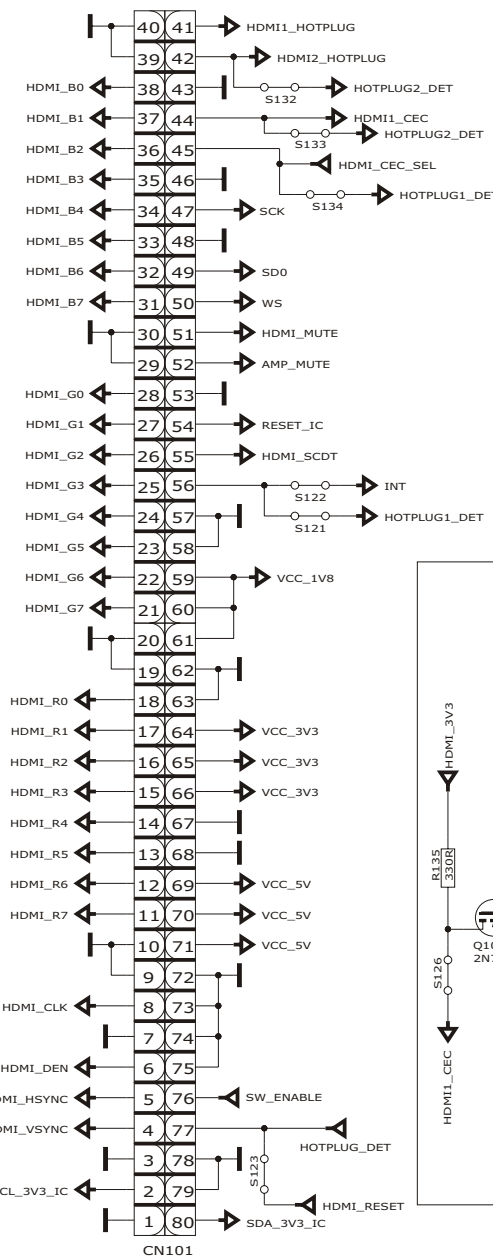
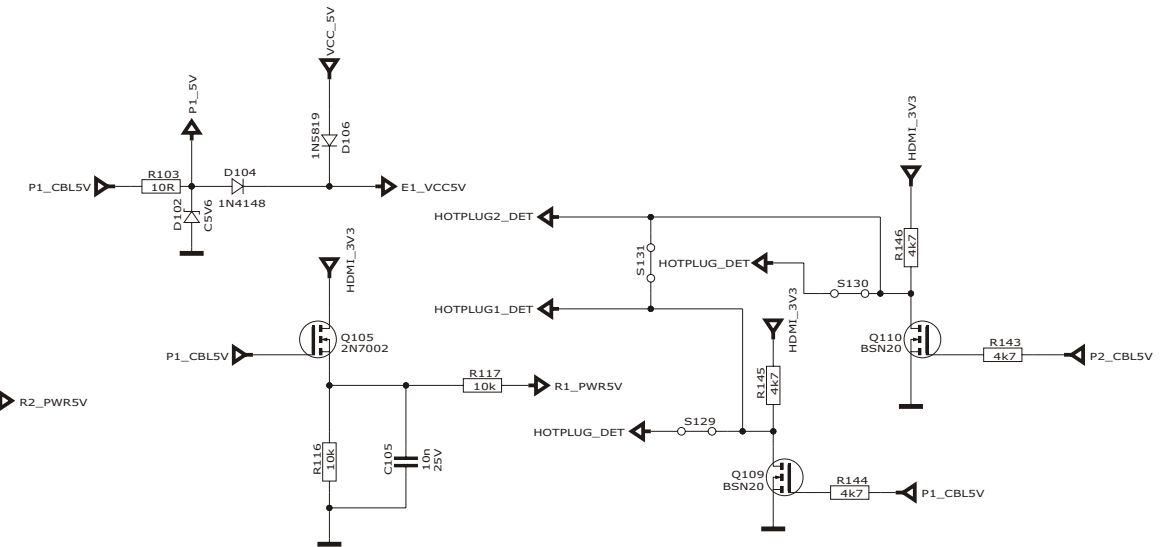
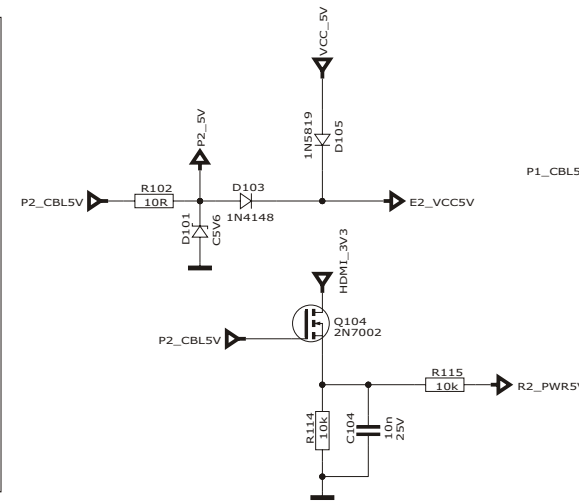
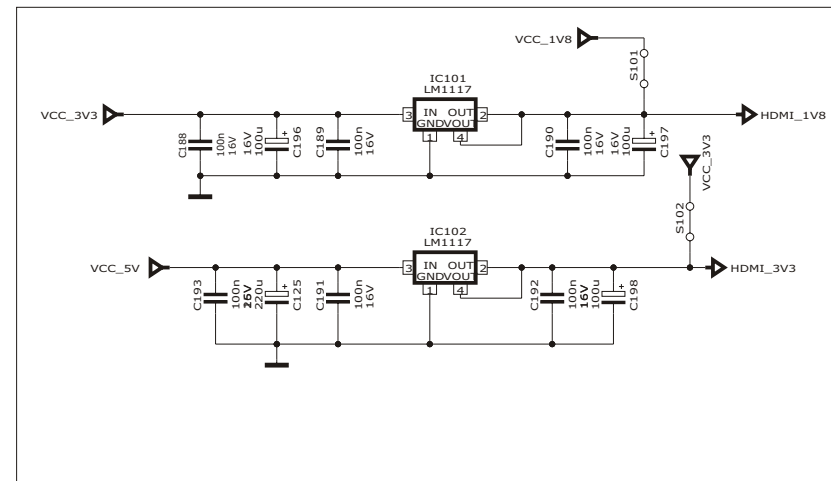
EXPLODED VIEW

HITACHI

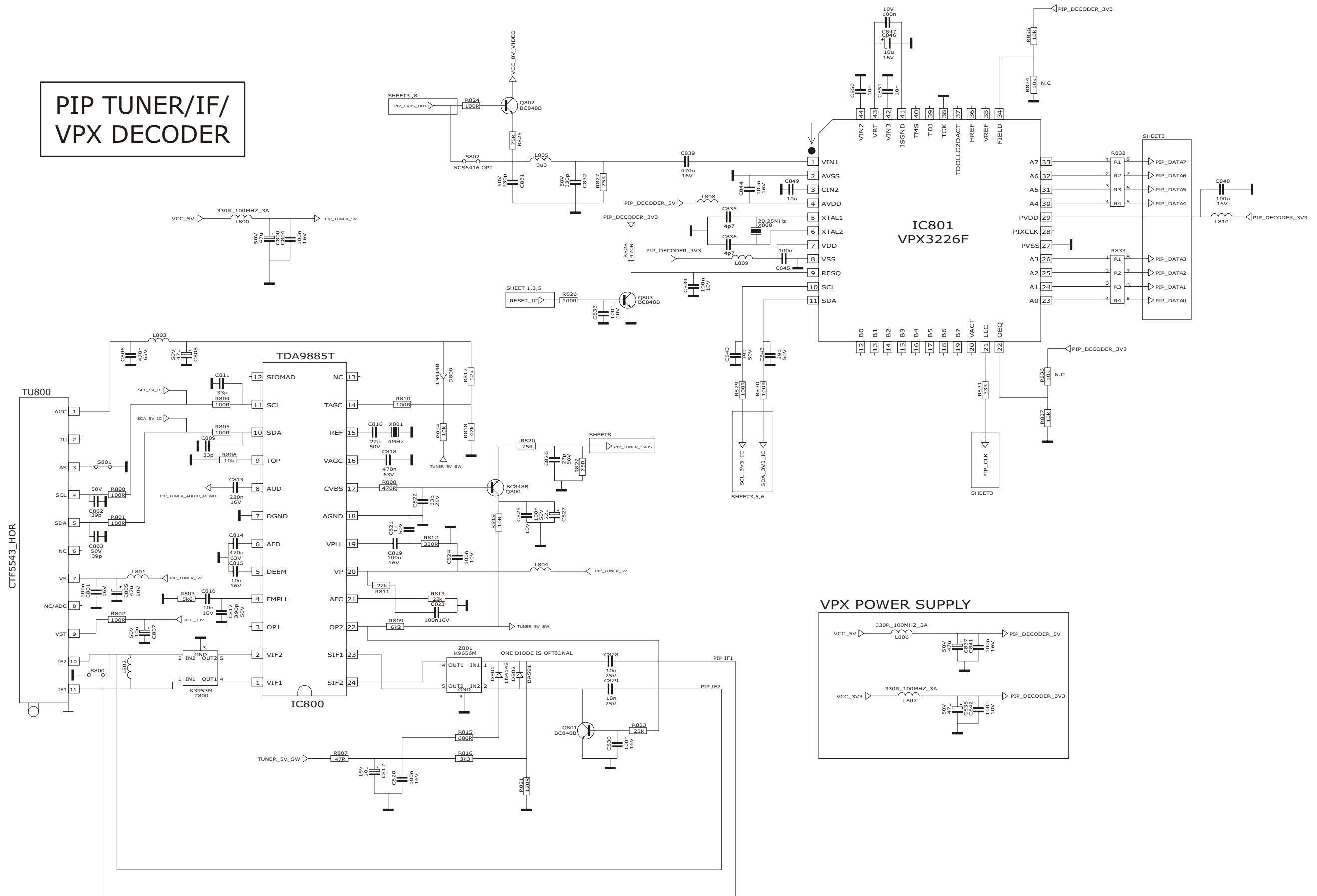
18. SCHEMATIC DIAGRAMS

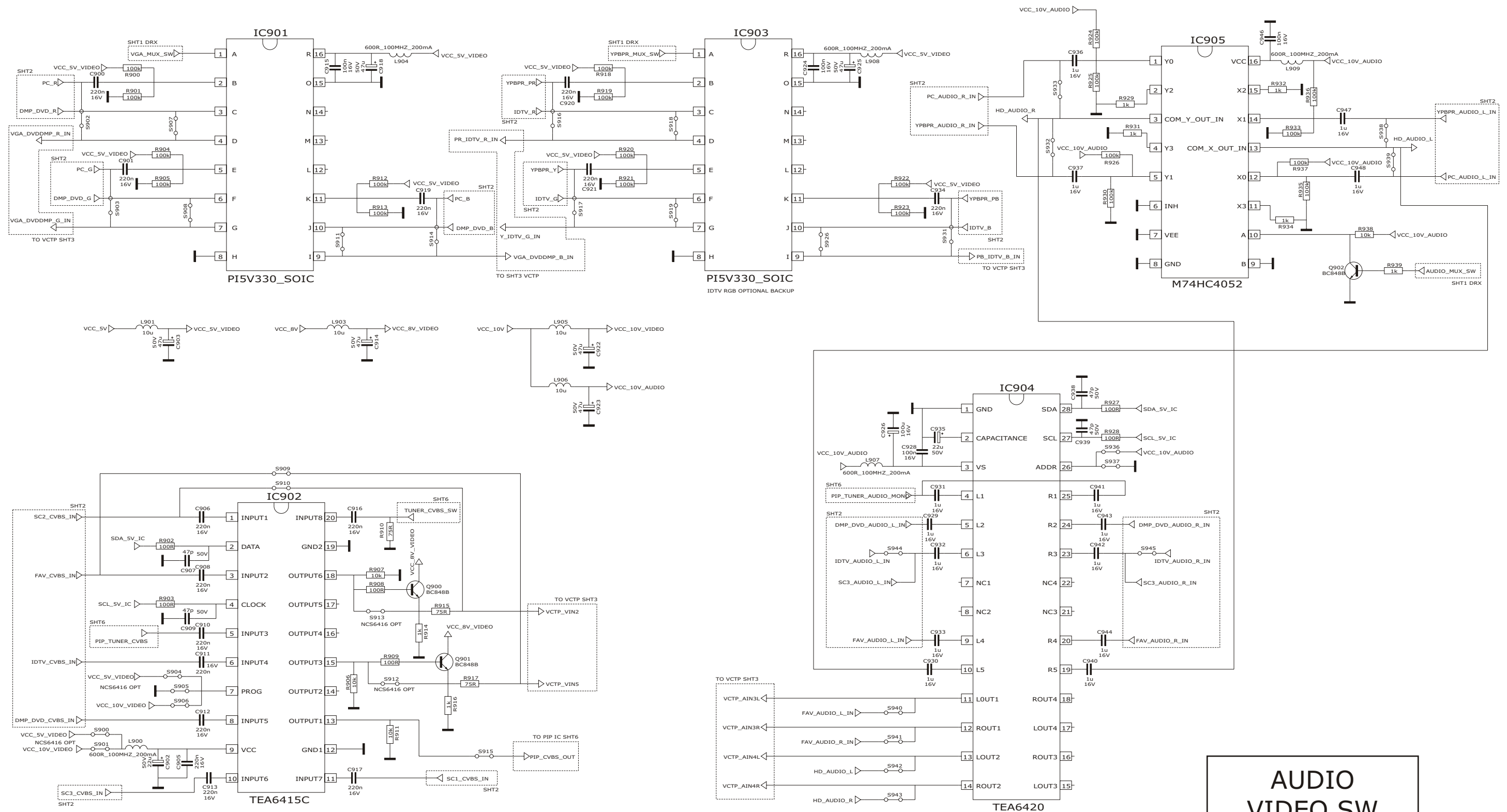


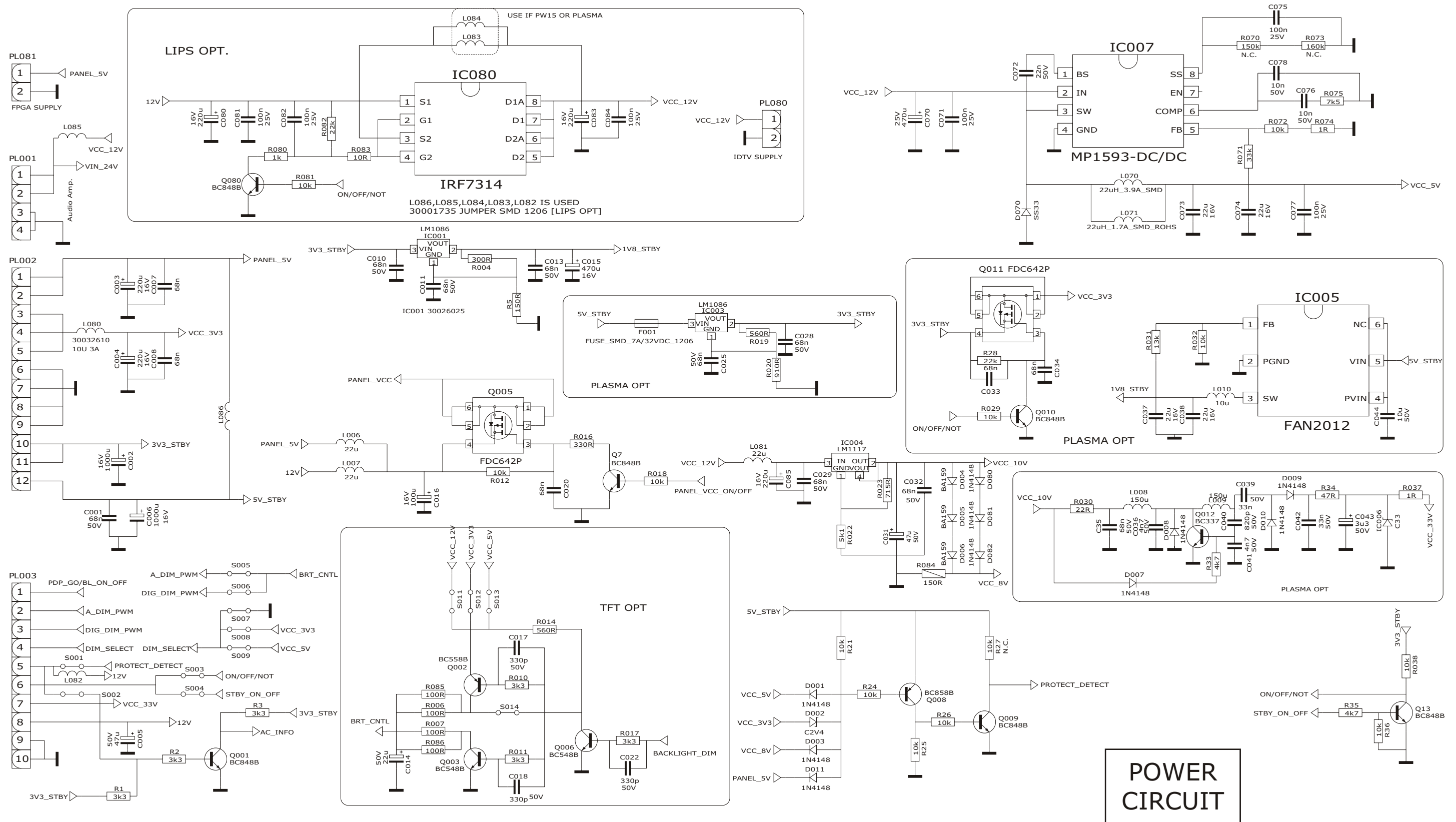


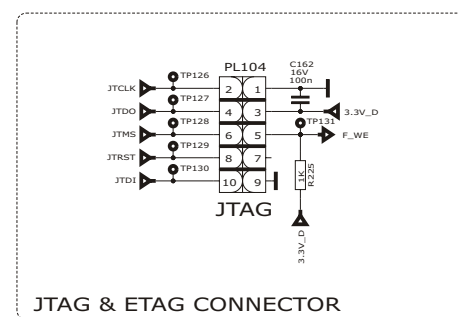
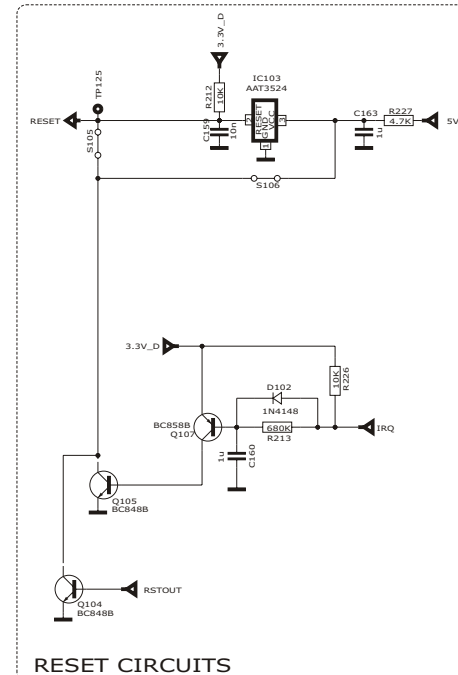
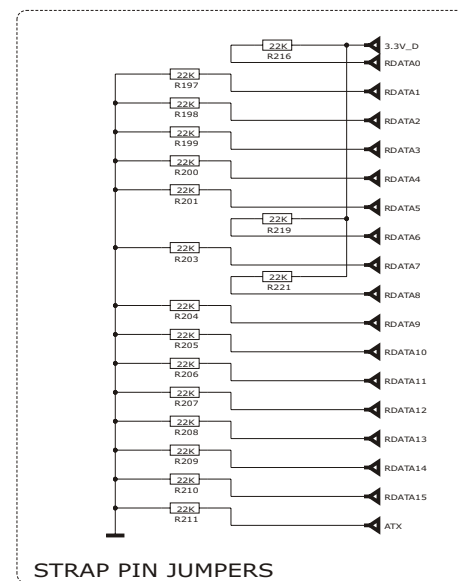
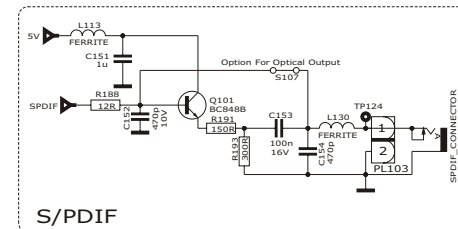
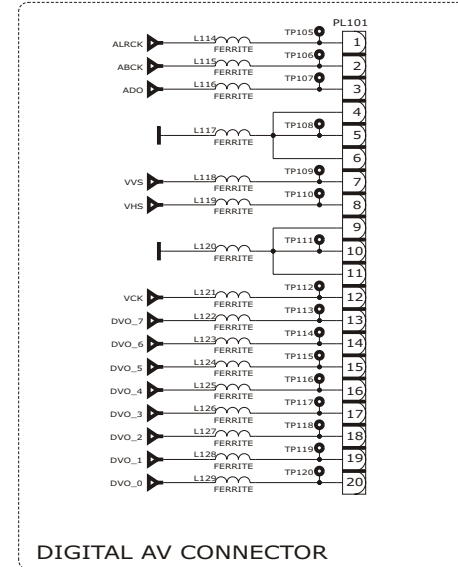
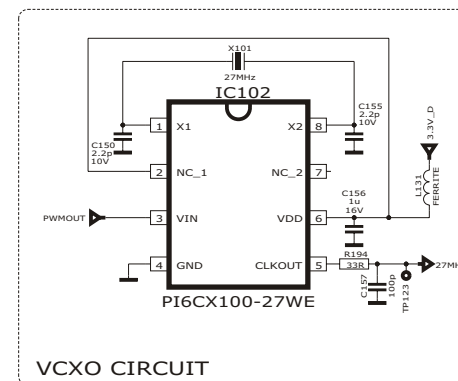
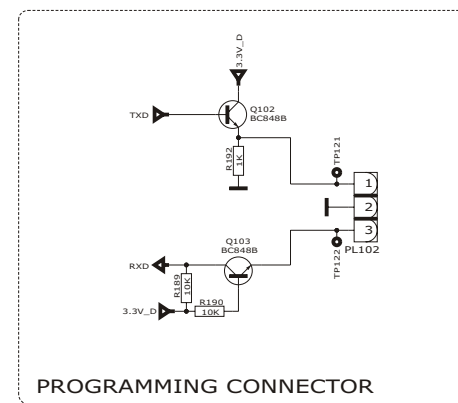
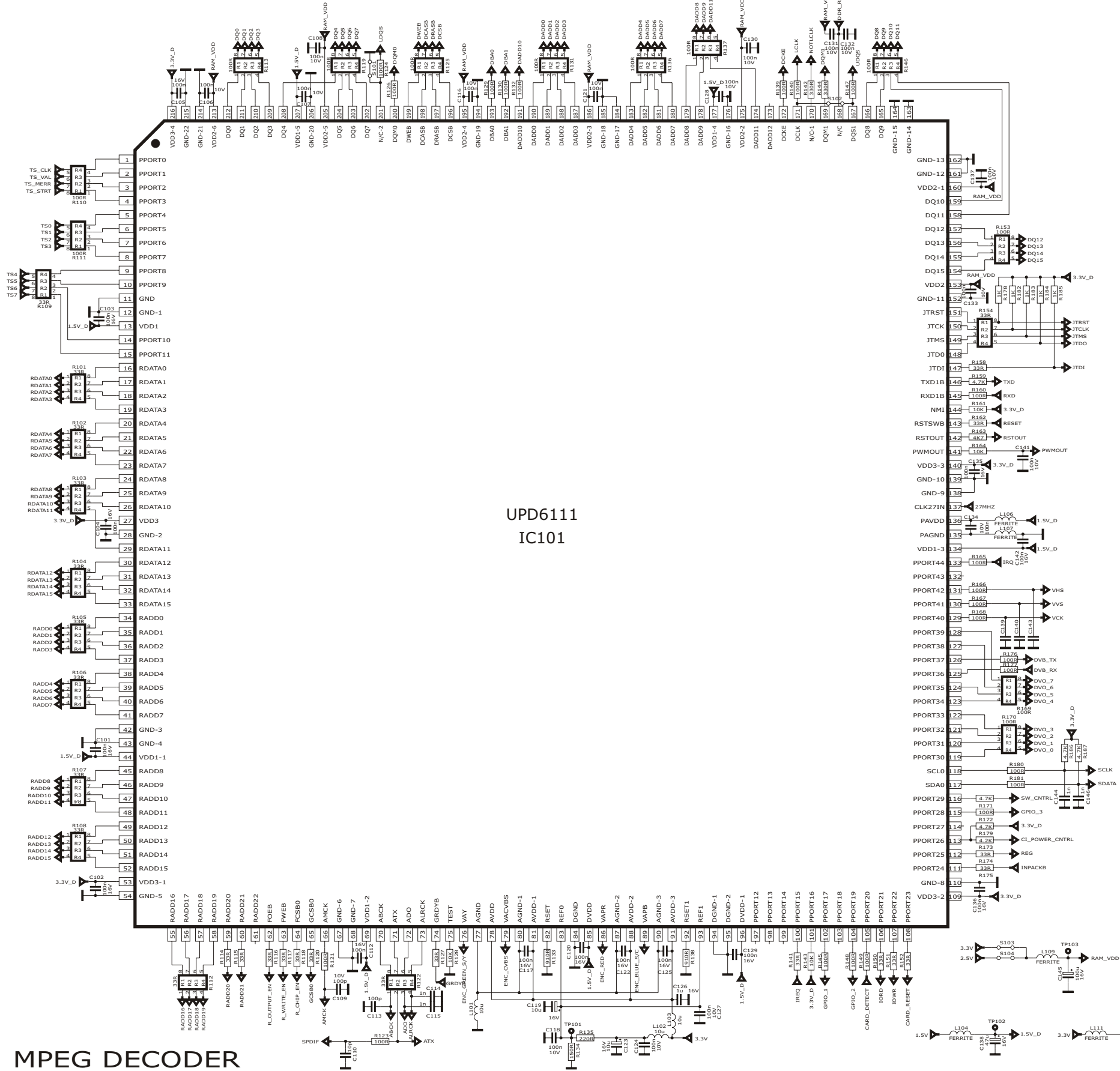


PIP TUNER/IF/ VPX DECODER





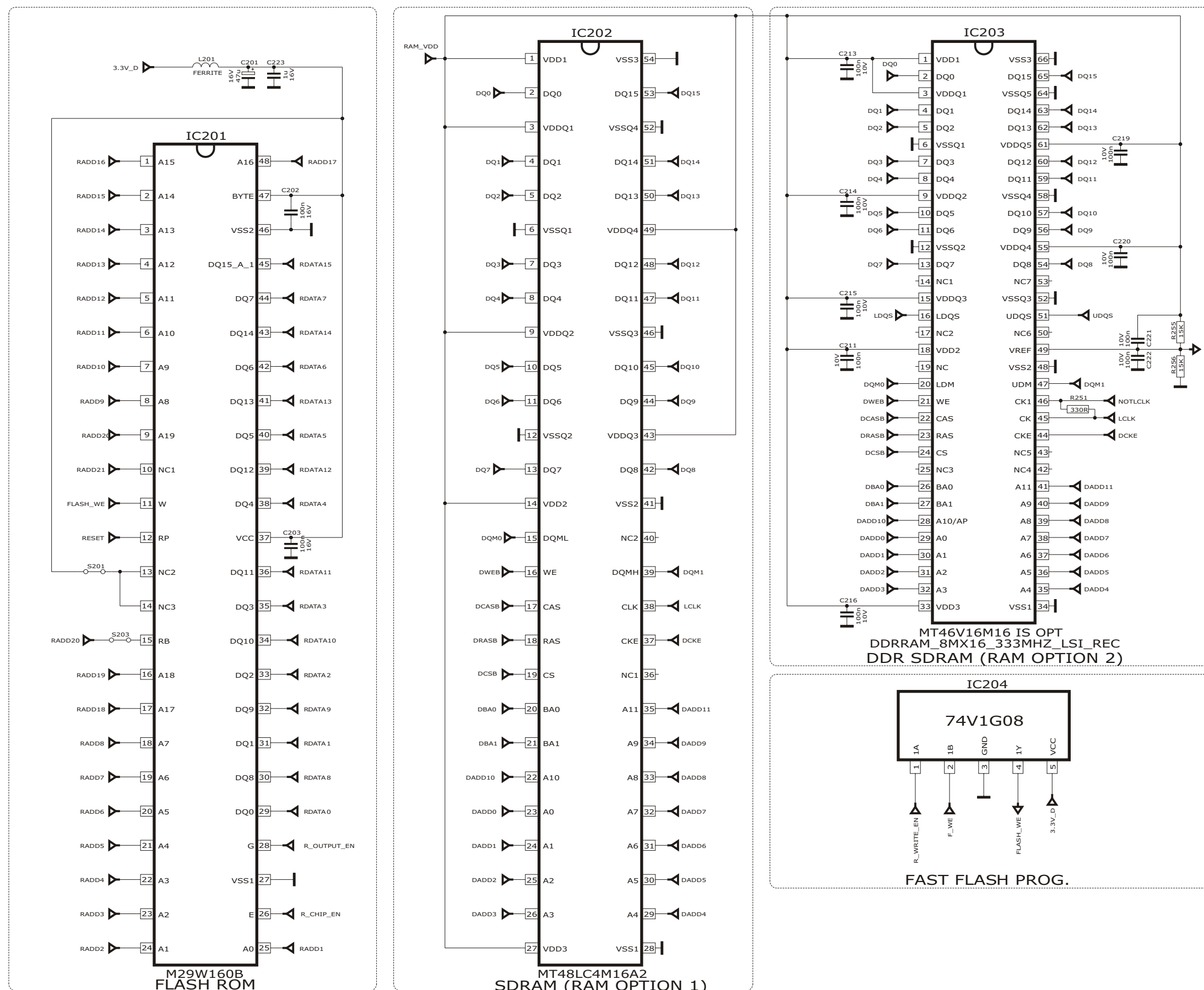


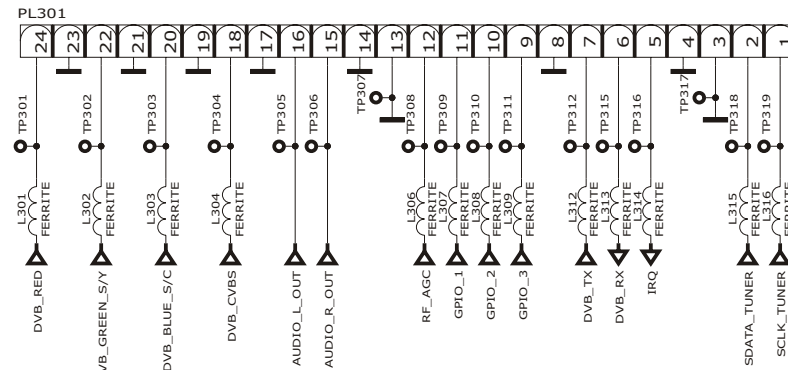


16MB1300

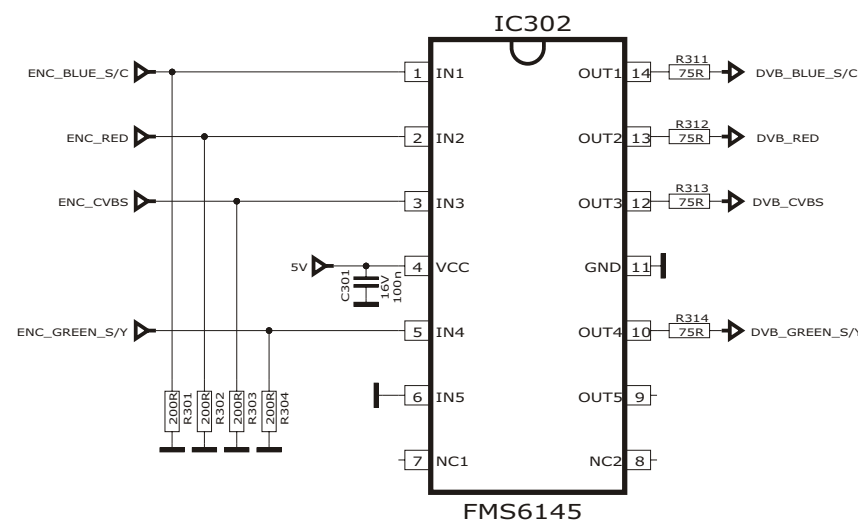
IDTV MODULE BOARD CIRCUIT - SHEET 1

HITACHI

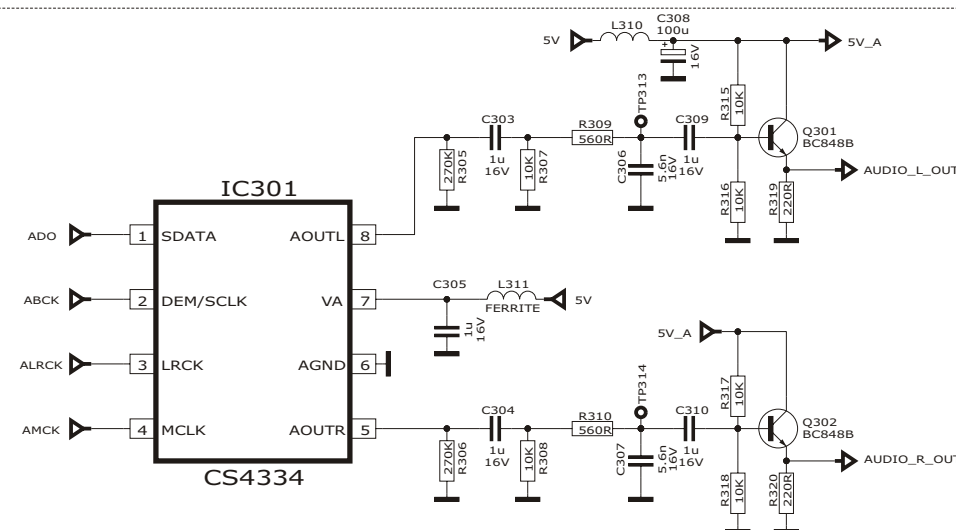




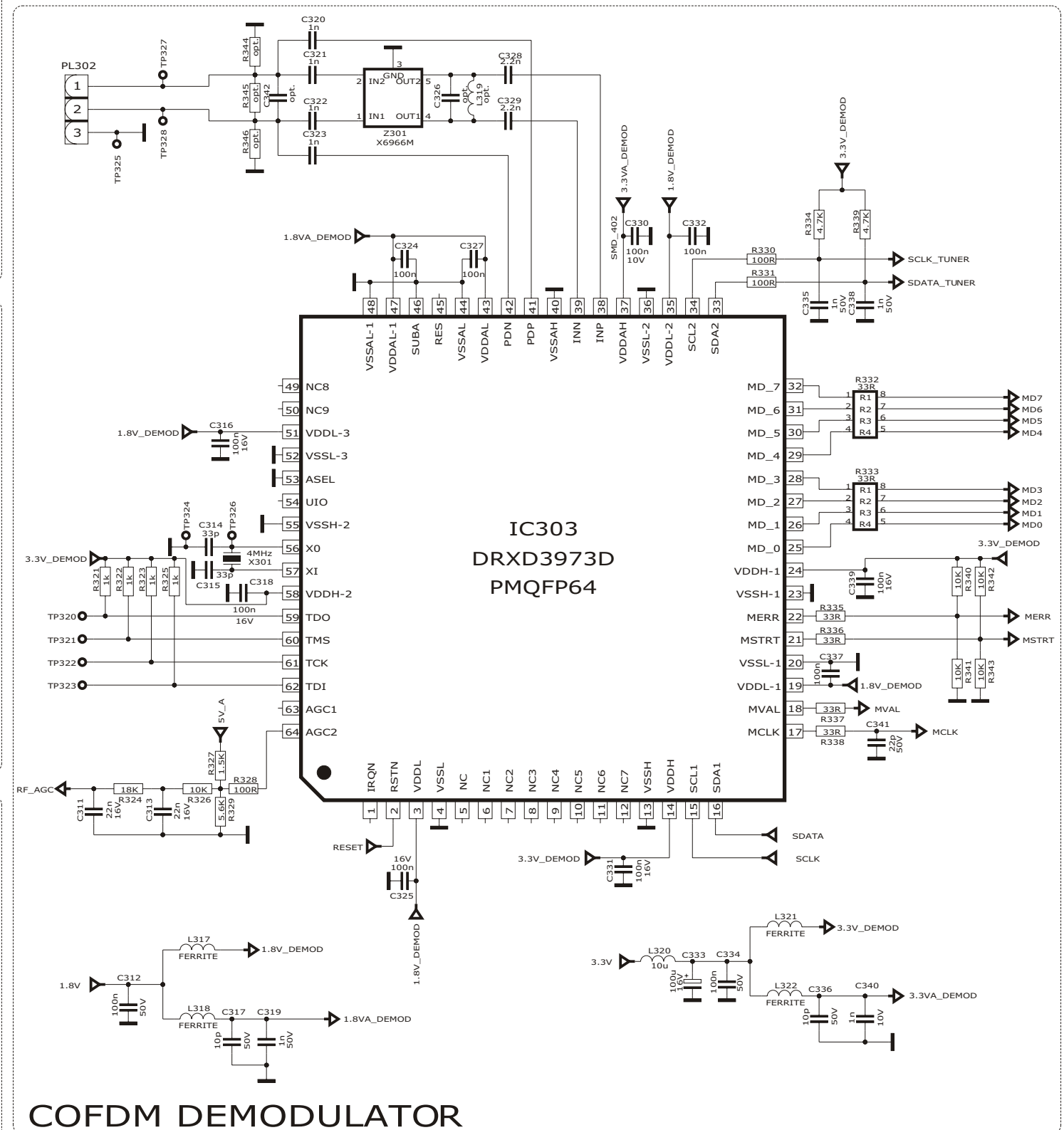
ANALOG AV CONNECTOR



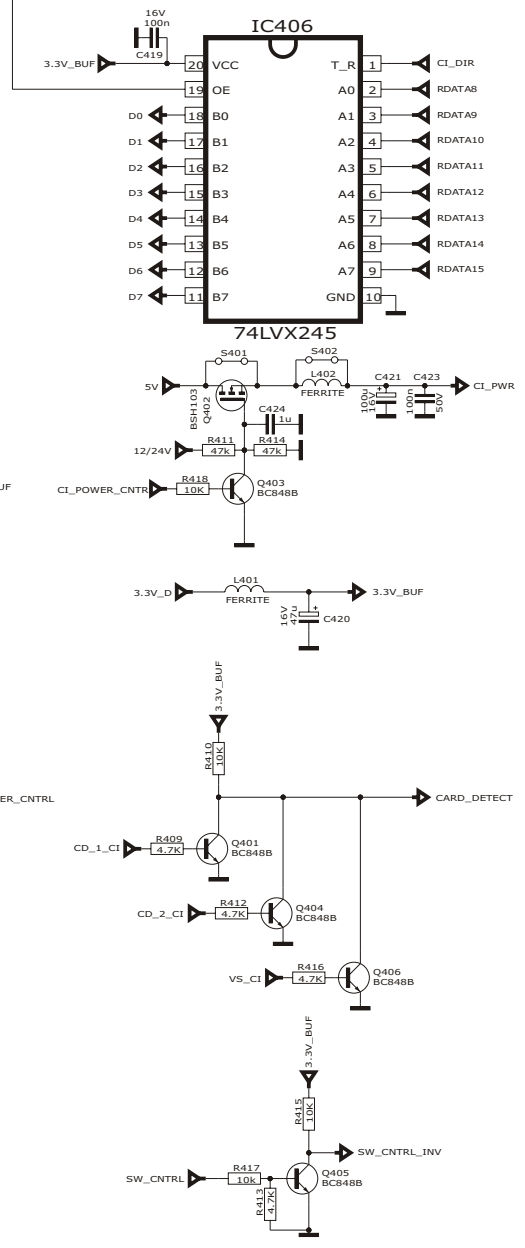
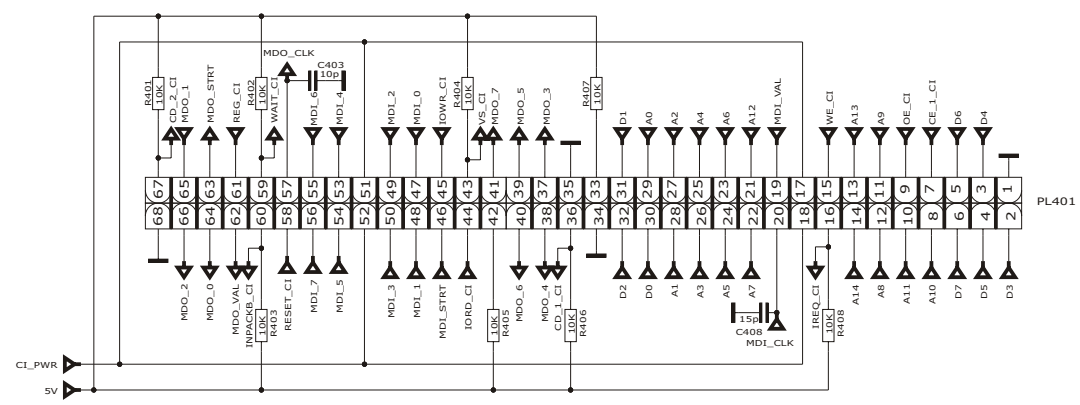
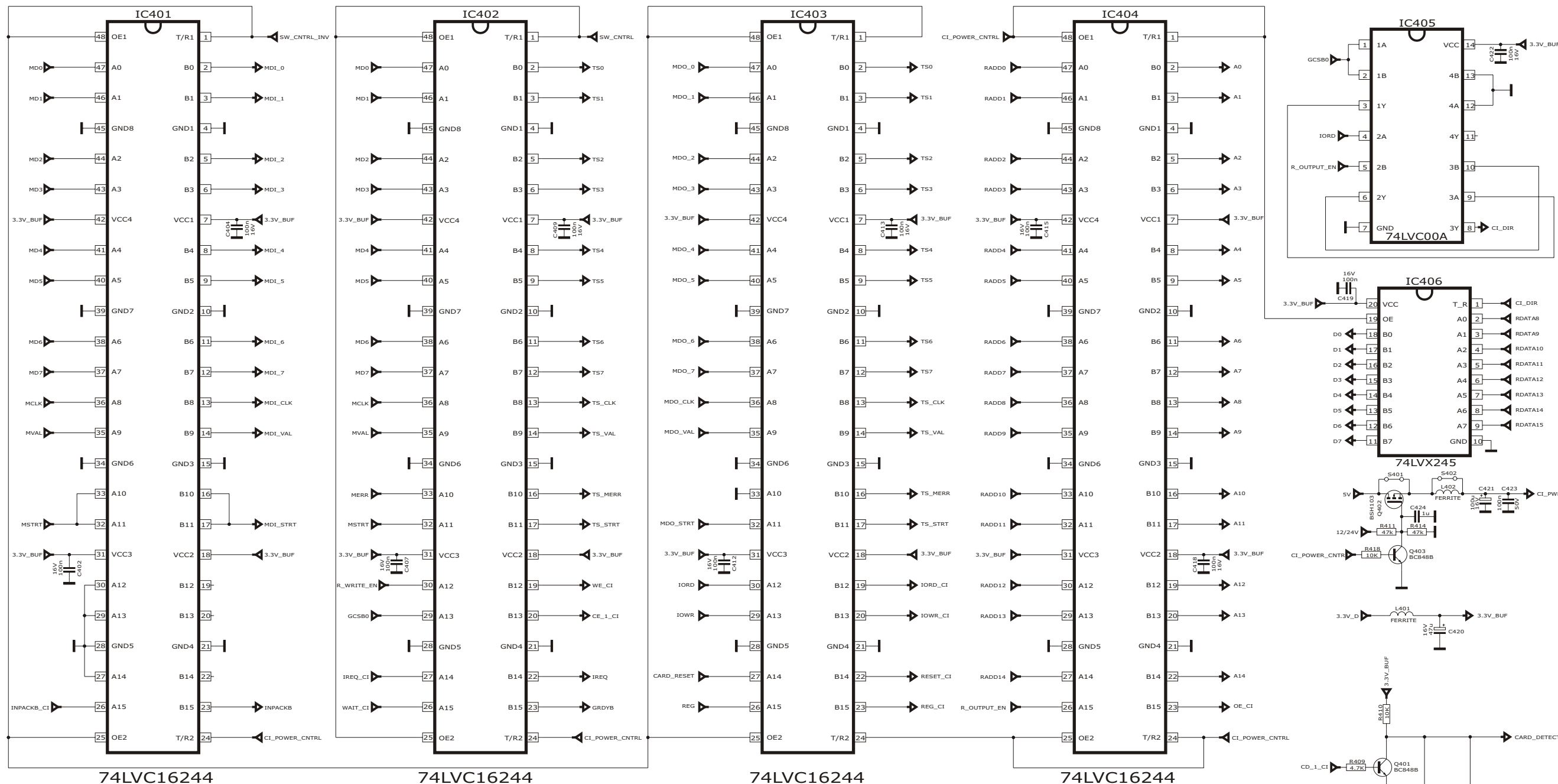
VIDEO AMPLIFIER



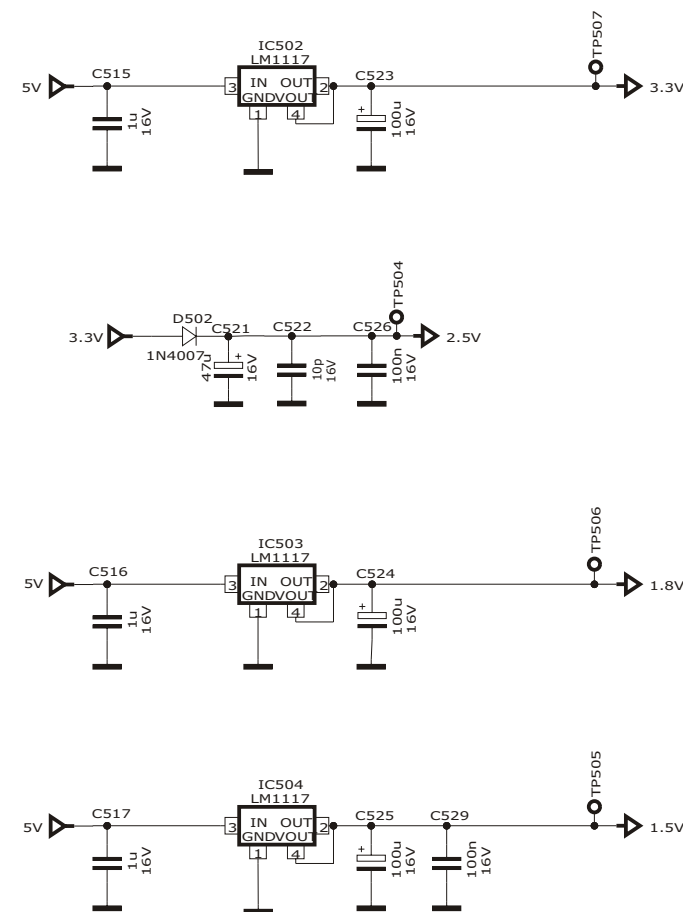
AUDIO DAC



COFDM DEMODULATOR

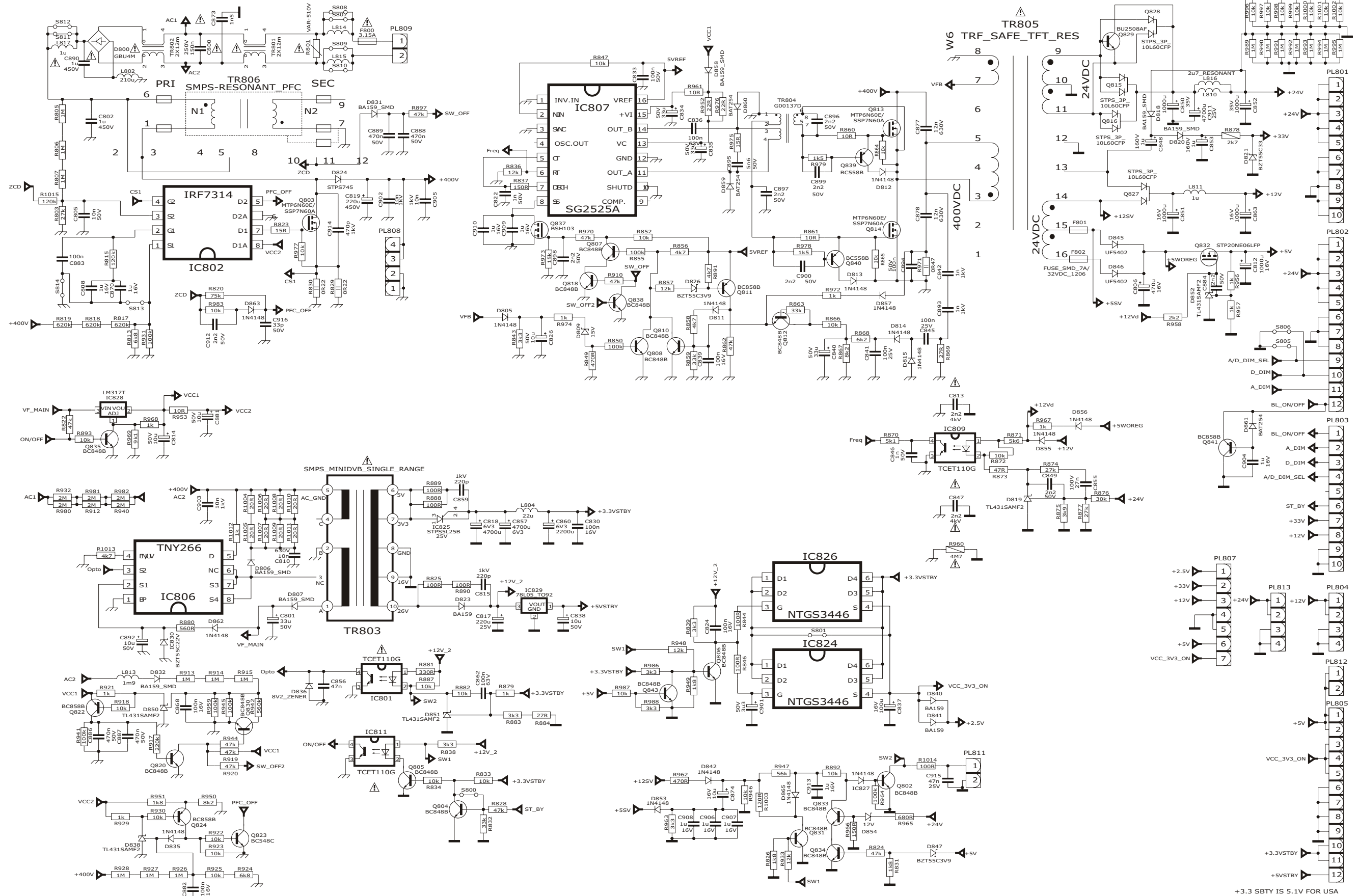


PCMCIA
INTERFACE



HITACHI

[For 32LD8D20EA, 32LD8D20UA and 37LD8D20E models]

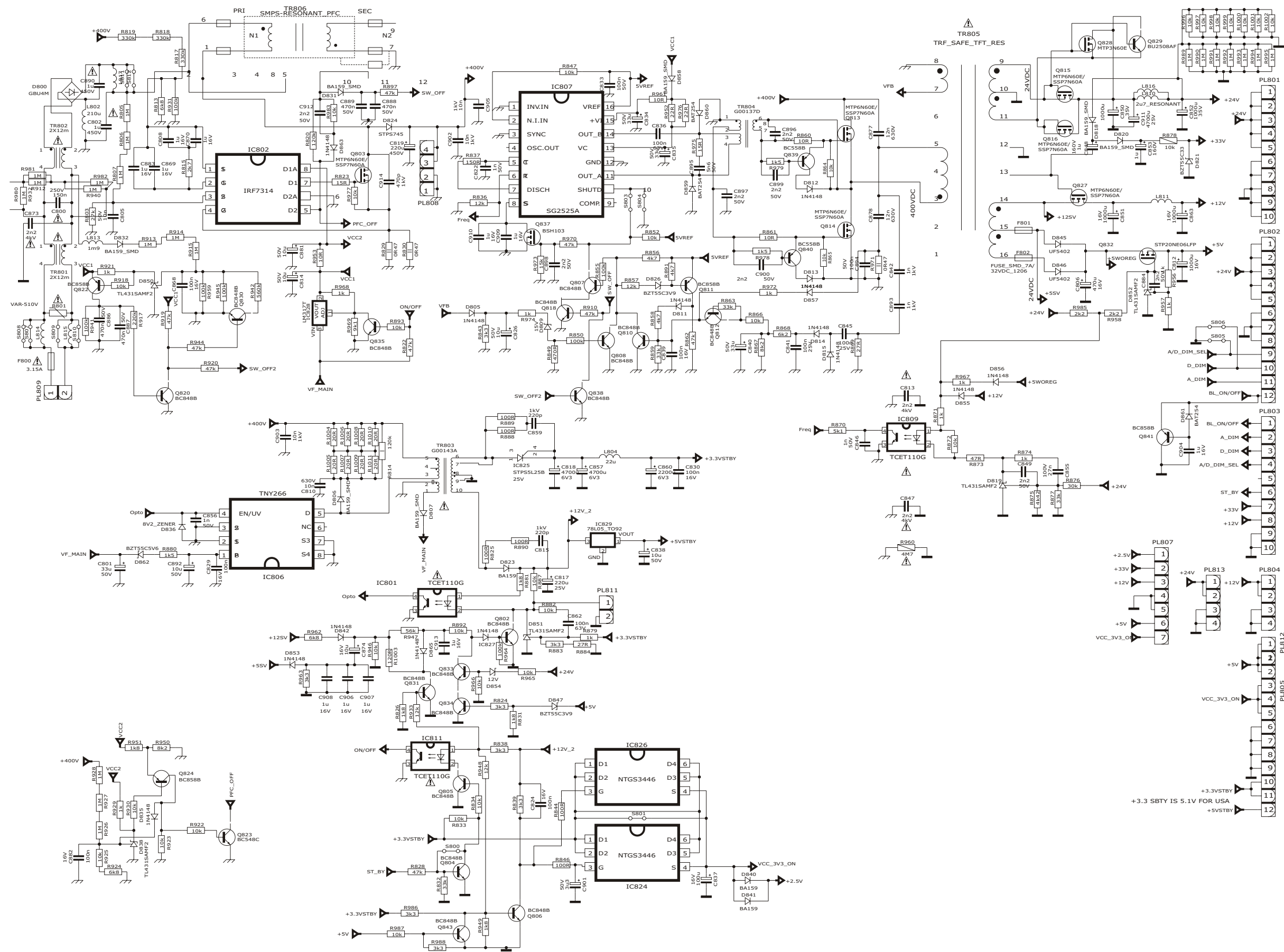


17PW20

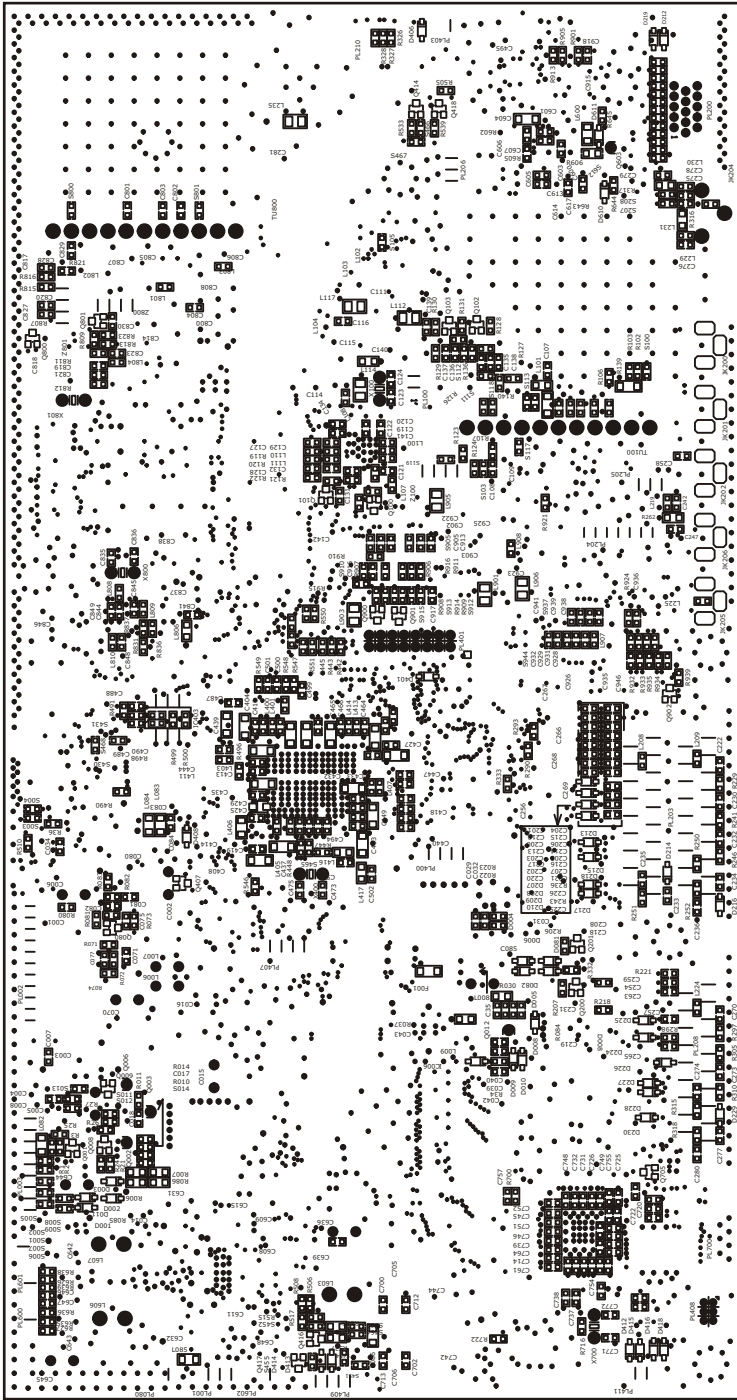
RESONANT MODE TFT POWER BOARD CIRCUIT

HITACHI

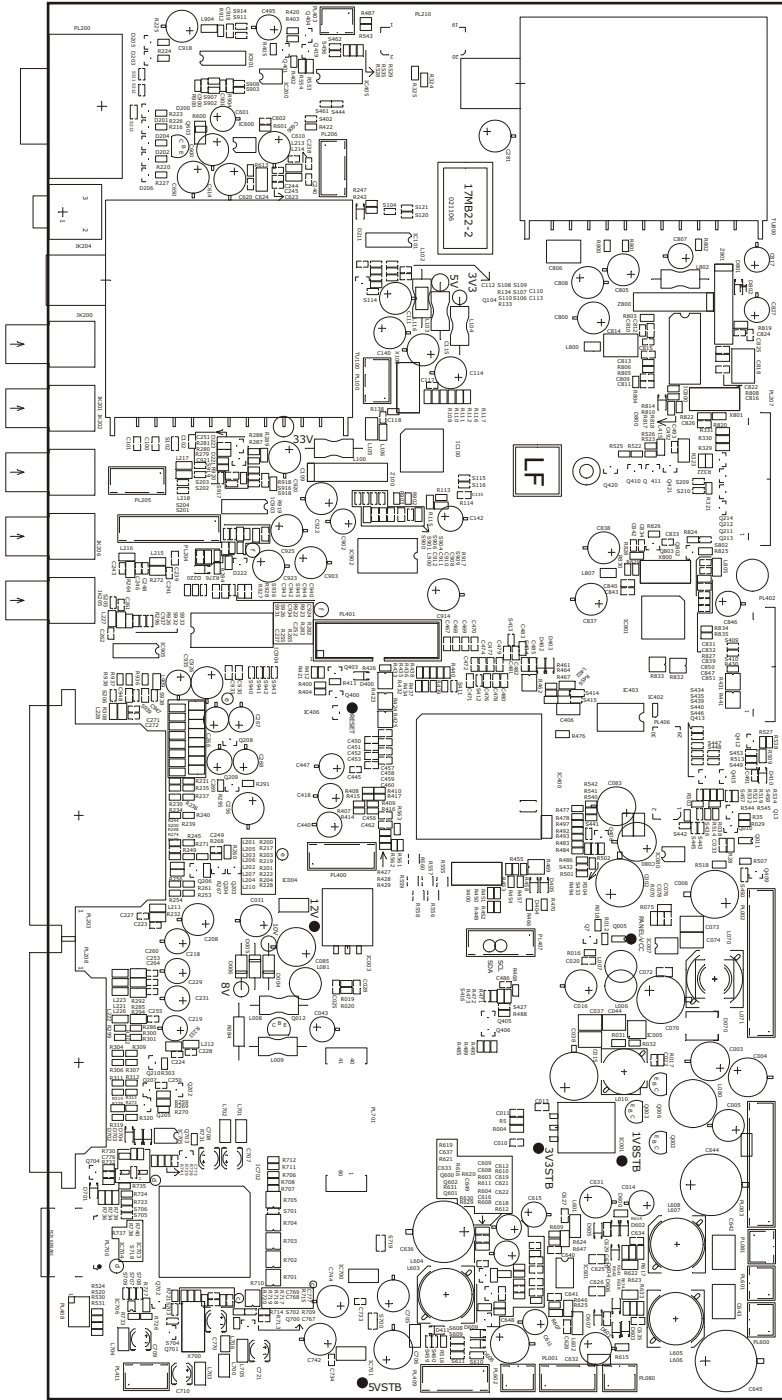
[For 32LD8D20E, 32LD8D20U, 37LD8D20U and 37LD8D20UA models]



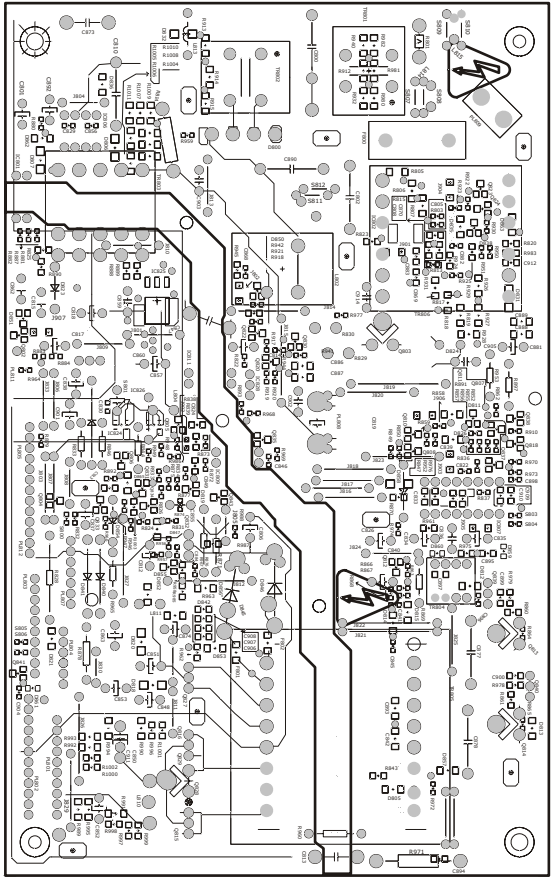
19. PCB Layout Diagrams [17PW15-9 POWER BOARD used in 32LD8D20E, 32LD8D20U, 37LD8D20U and 37LD8D20UA models ONLY]



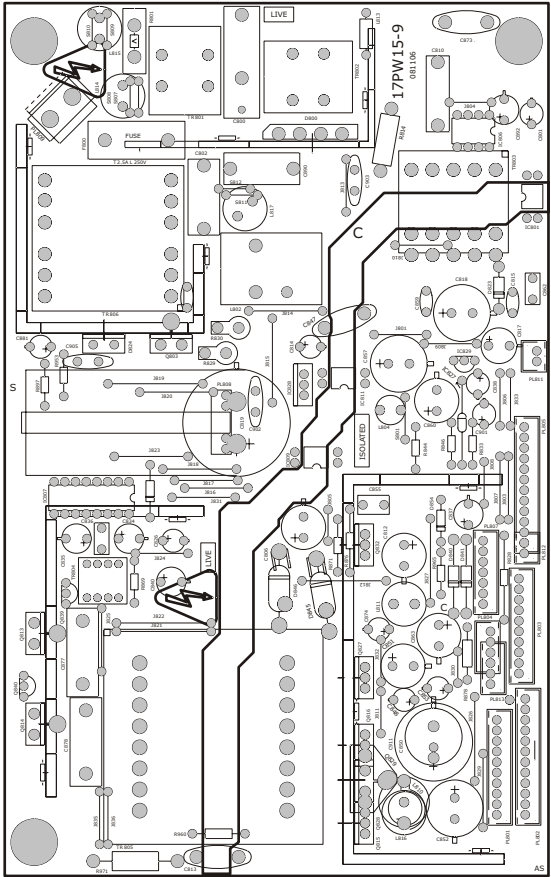
SOLDER SIDE (BOTTOM)
MAIN BOARD (17MB22-2)



COMPONENT SIDE (TOP)

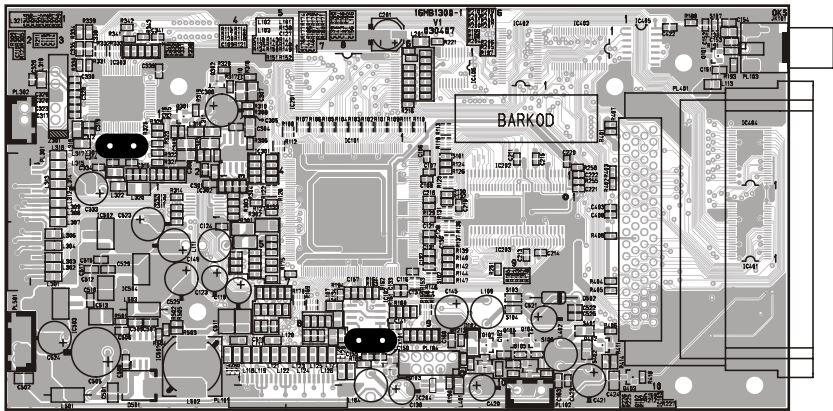


SOLDER SIDE (BOTTOM)



COMPONENT SIDE (TOP)

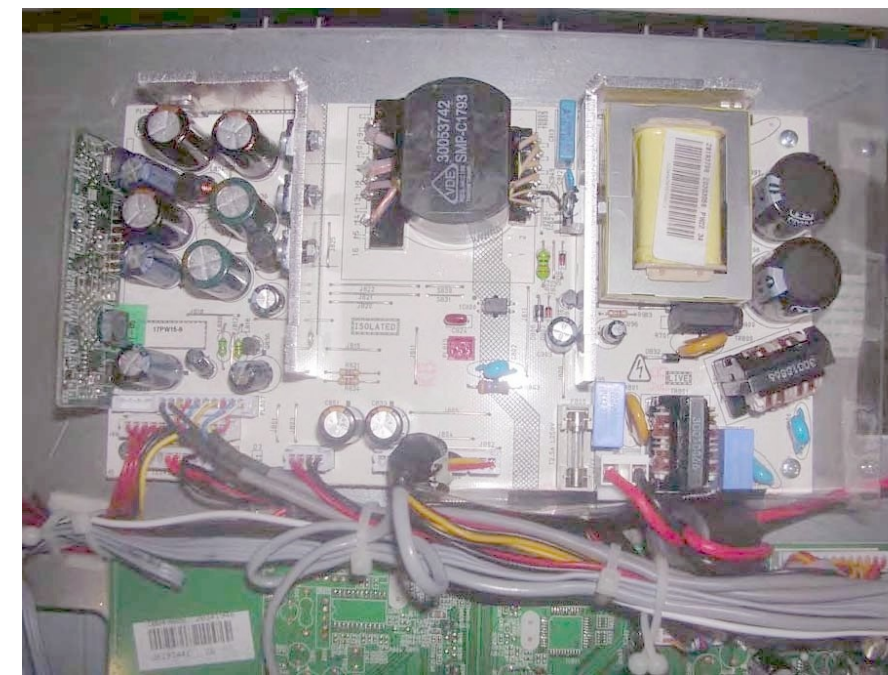
POWER BOARD (17MB15-9)



COMPONENT SIDE (TOP)
IDTV MODULE BOARD (16MB1300E1)



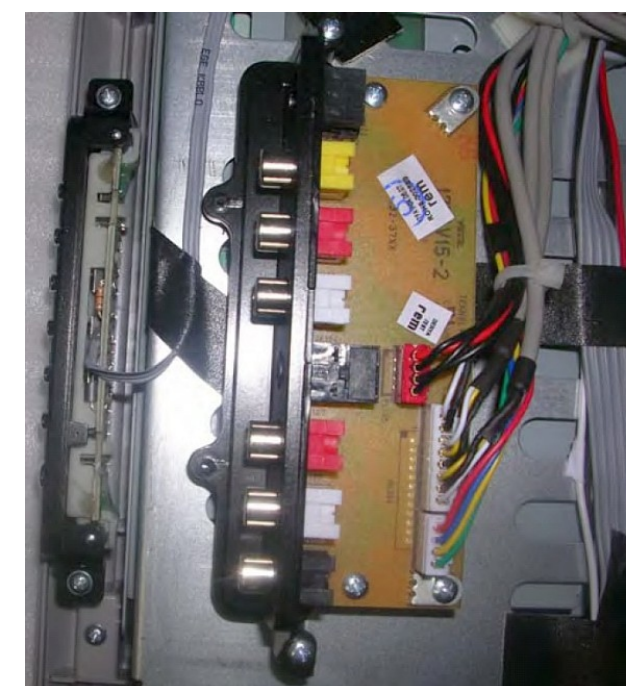
MAIN BOARD (17MB22-2)



POWER BOARD (17PW15-9)



TDM1300 IDTV MODULE
BOARD (16MB1300-E1)



FAV BOARD (17FAV15)

HITACHI

Hitachi, Ltd. Tokyo, Japan

International Sales Division

THE HITACHI ATAGO BUILDING,

No. 15-12 Nishi Shinbashi, 2 - Chome,

Minato - Ku, Tokyo 105-8430, Japan.

Tel: 03 35022111

HITACHI EUROPE LTD,

Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire
SL6 8YA

UNITED KINGDOM

Tel: 01628 643000

Fax: 01628 643400

Email: consumer-service@hitachi-eu.com

HITACHI EUROPE S.A.

364 Kifissias Ave. & 1, Delfon Str.
152 33 Chalandri
Athens

GREECE

Tel: 1-6837200

Fax: 1-6835964

Email: service.hellas@hitachi-eu.com

HITACHI EUROPE GmbH

Munich Office
Dornacher Strasse 3
D-85622 Feldkirchen bei München

GERMANY

Tel: +49-89-991 80-0

Fax: +49-89-991 80-224

Hotline: +49-180-551 25 51 (12ct/min)

Email: HSE-DUS.service@hitachi-eu.com

HITACHI EUROPE S.A.

Gran Via Carlos III, 86, planta 5
Edificios Trade - Torre Este
08028 Barcelona

SPAIN

Tel: +34 93 409 2550

Fax: +34 93 491 3513

Email: atencion.cliente@hitachi-eu.com

HITACHI EUROPE srl

Via Tommaso Gulli N.39, 20147
Milano, Italia

ITALY

Tel: +39 02 487861

Tel: +39 02 38073415 Servizio Clienti

Fax: +39 02 48786381/2

Email: customerservice.italy@hitachi-eu.com

HITACHI Europe AB

Box 77 S-164 94 Kista

SWEDEN

Tel: +46 (0) 8 562 711 00

Fax: +46 (0) 8 562 711 13

Email: csgswe@hitachi-eu.com

HITACHI EUROPE S.A.S

Lyon Office
B.P. 45, 69671 BRON CEDEX

FRANCE

Tel: +33 04 72 14 29 70

Fax: +33 04 72 14 29 99

Email: france.consommateur@hitachi-eu.com

HITACHI EUROPE LTD (Norway) AB

STRANDVEIEN 18

1366 Lysaker

NORWAY

Tel: 67 5190 30

Fax: 67 5190 32

Email: csgnor@hitachi-eu.com

HITACH EUROPE AB

Egebækgård
Egebækvej 98
DK-2850 Nærum

DENMARK

Tel: +45 43 43 6050

Fax: +45 43 60 51

Email: csgnor@hitachi-eu.com

HITACHI EUROPE AB

Neopoli / Niemenkatu 73

FIN-15140 Lahti

FINLAND

Tel : +358 3 8858 271

Fax: +358 3 8858 272

Email: csgnor@hitachi-eu.com

Hitachi Europe Ltd

Bergensesteenweg 421
1600 Sint-Pieters-Leeuw

BELGIUM

Tel: +32 2 363 99 01

Fax: +32 2 363 99 00

Email: sofie.van.bom@hitachi-eu.com

HITACHI EUROPE LTD

Na Sychrove 975/8

101 27 Praha 10 - Bohdalec

CZECH REPUBLIC

Tel: +420 267 212 383

Fax: +420 267 212 385

Email: csgnor@hitachi-eu.com

www.hitachidigitalmedia.com